MatRaptor: A Sparse-Sparse Matrix Multiplication Accelerator Based On Row-Wise Product

Nitish Srivastava*, Hanchen Jin, Jie Liu,
David Albonesi and Zhiru Zhang

School of ECE, Cornell University
***now at Google**

Applications of Sparse-Sparse Matrix Multiplication

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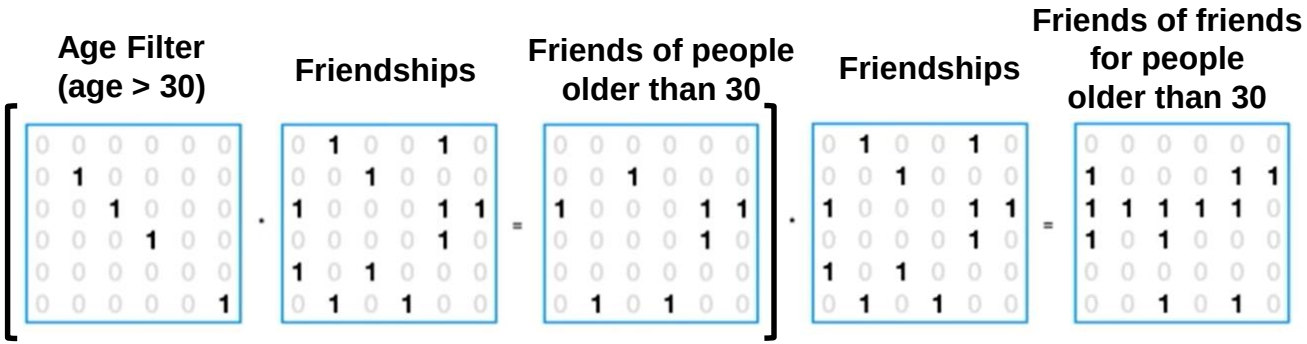
Graph Computing

(e.g. database searches in graphs [1])



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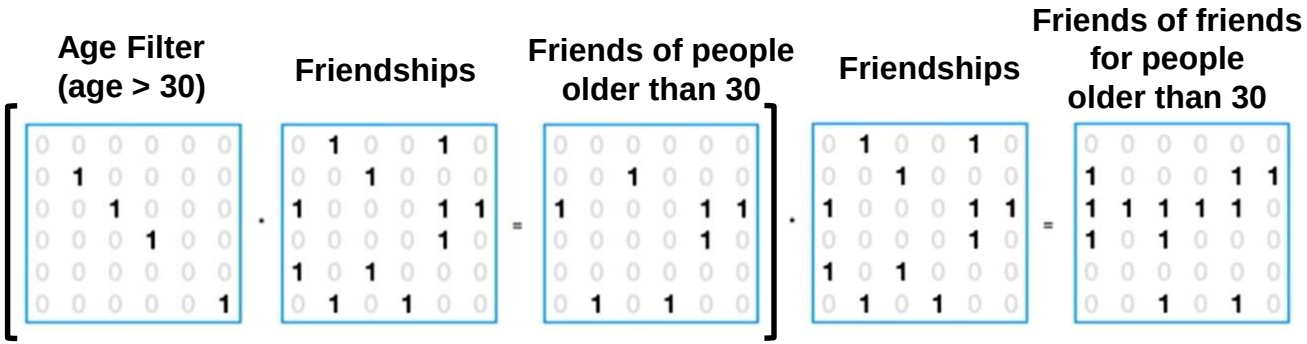

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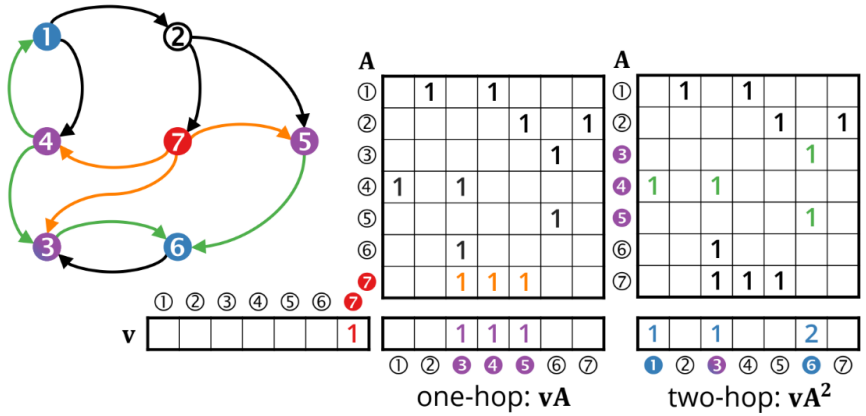
Graph Traversals [2]



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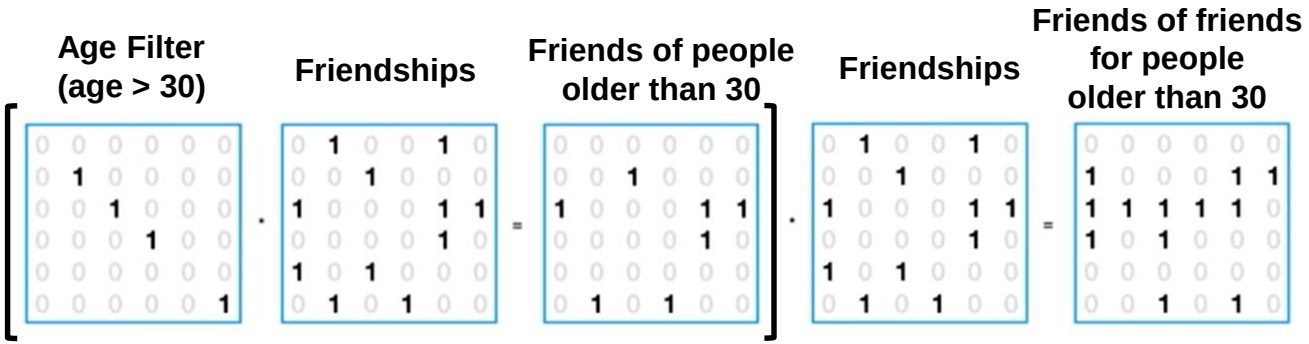

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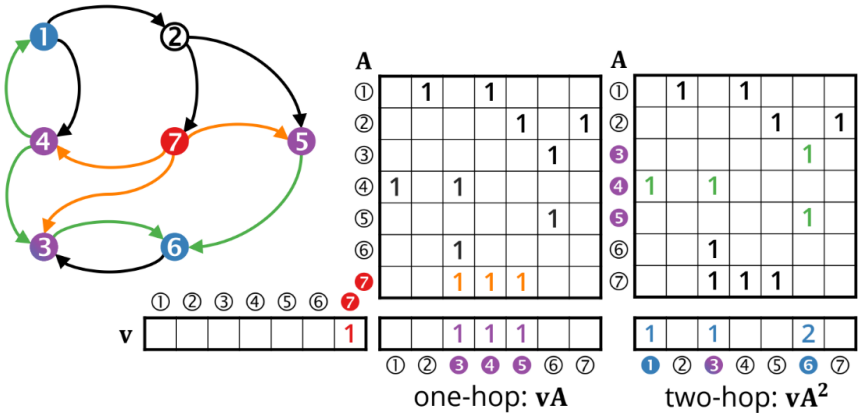
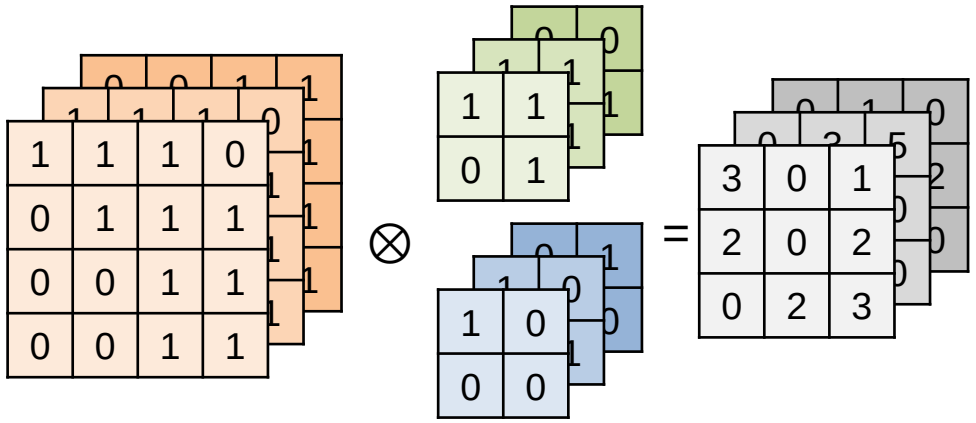


Compressed Neural Networks



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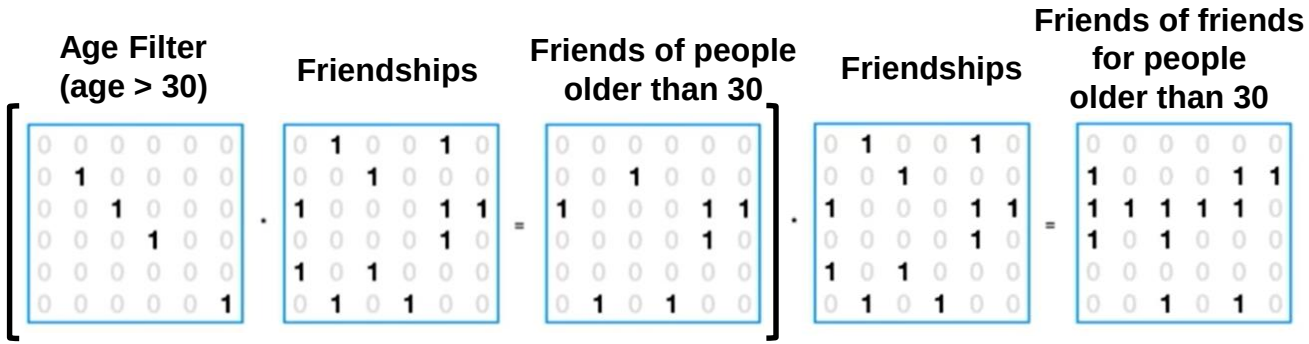

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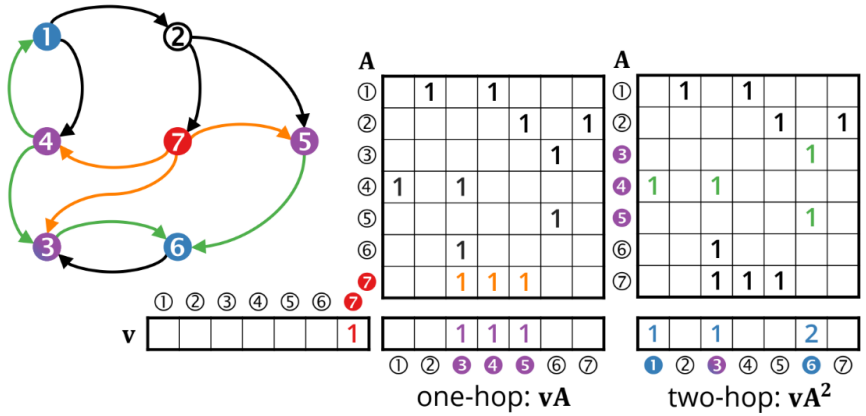

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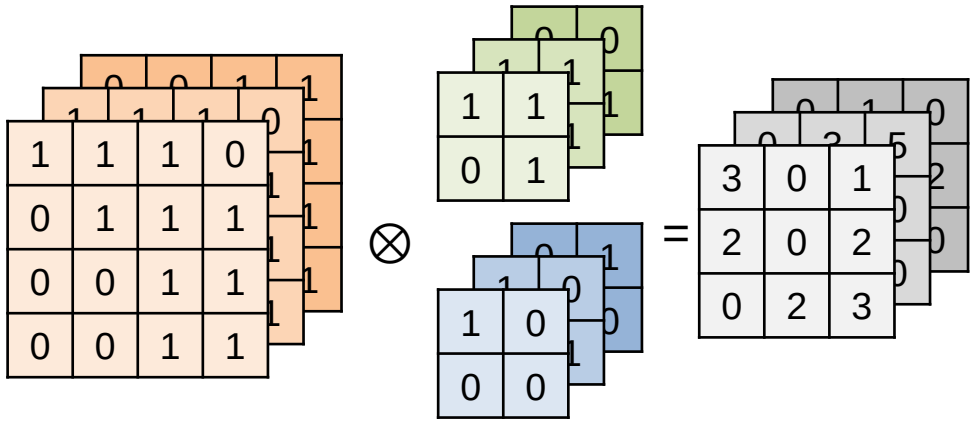
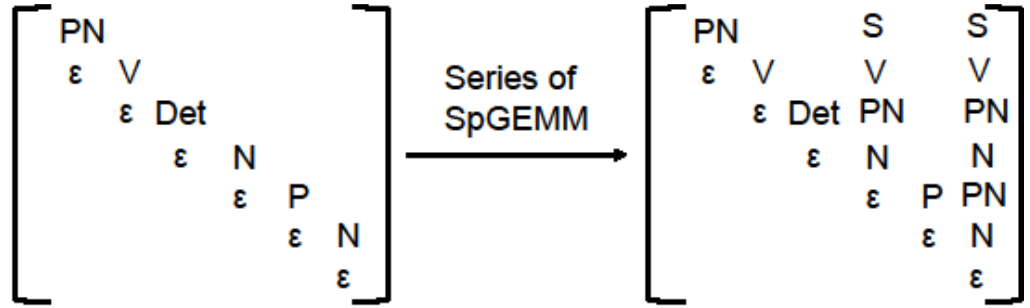


Engineering Applications
(e.g. Grammar Parsing [3])



Simple Sentence:
John (PN) sees (V) the (Det)
man (N) with (P) telescope (N)

Transitive Closure

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[2] J. R. Gilbert, S. Reinhardt, and V. B. Shah, "A Unified Framework for Numerical and Combinatorial Computing," Computing in Science & Engineering
[3] Penn, Gerald. "Efficient transitive closure of sparse matrices over closed semirings.", Theoretical Computer Science, 2006

Traditional Approaches: Inner Product [4]

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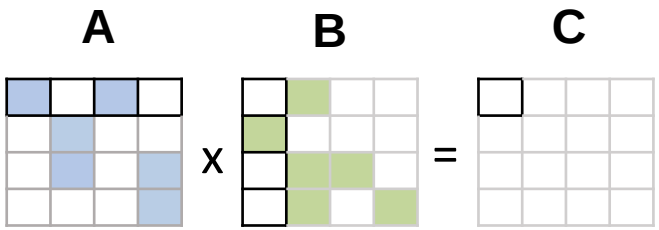

Inner Product

$$C[i,j] = \sum_{k} A[i,k] \cdot B[k,j]$$

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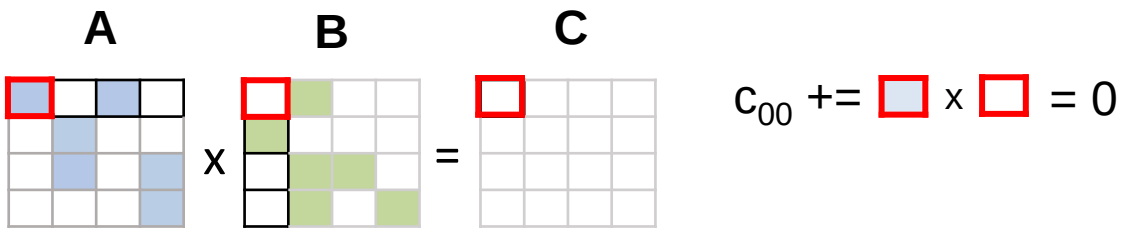

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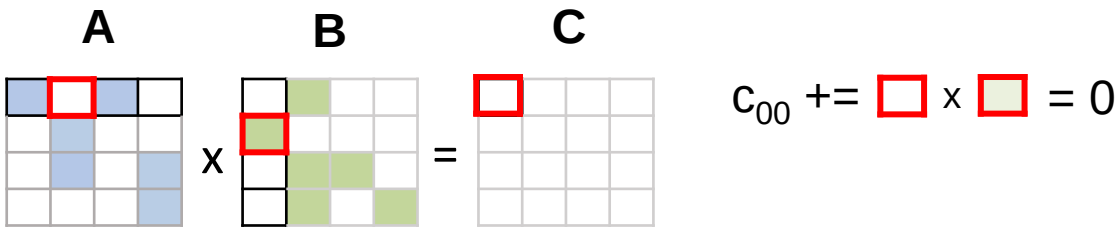

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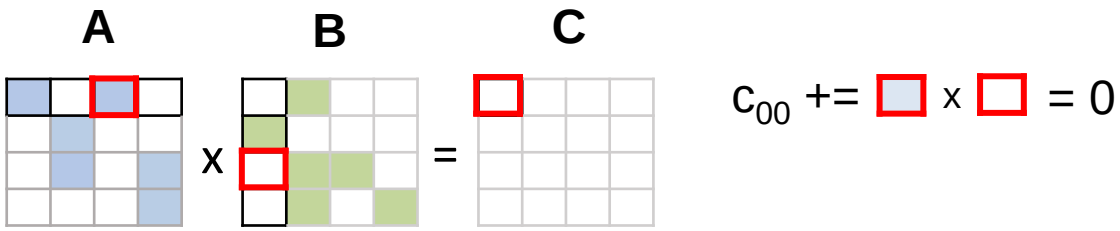

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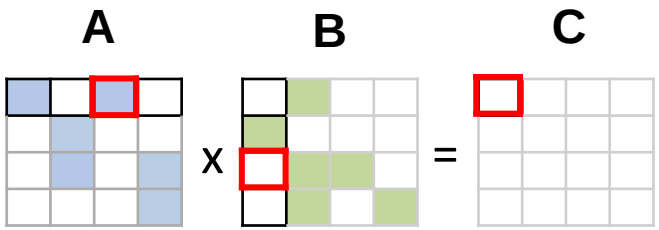

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3 operations to produce a 0

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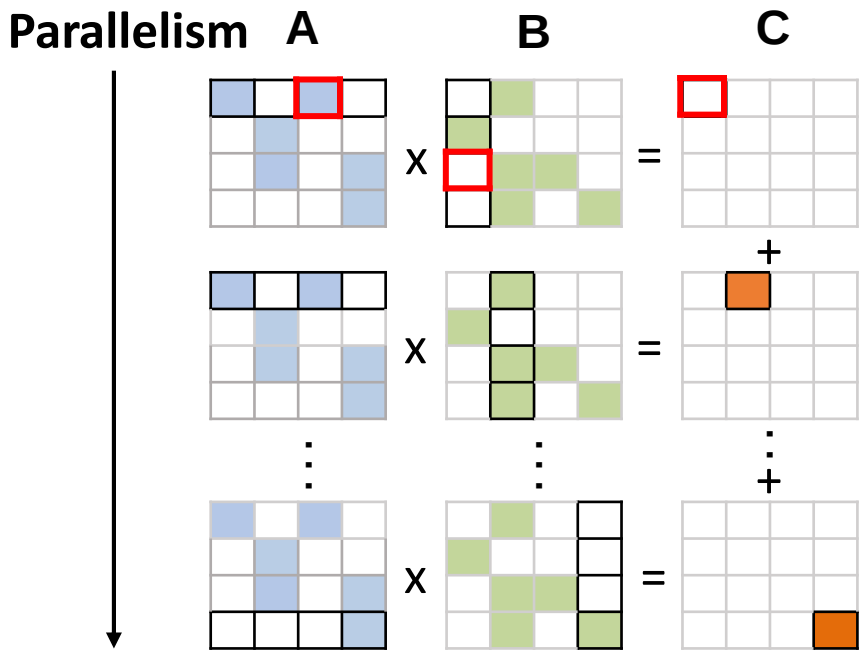

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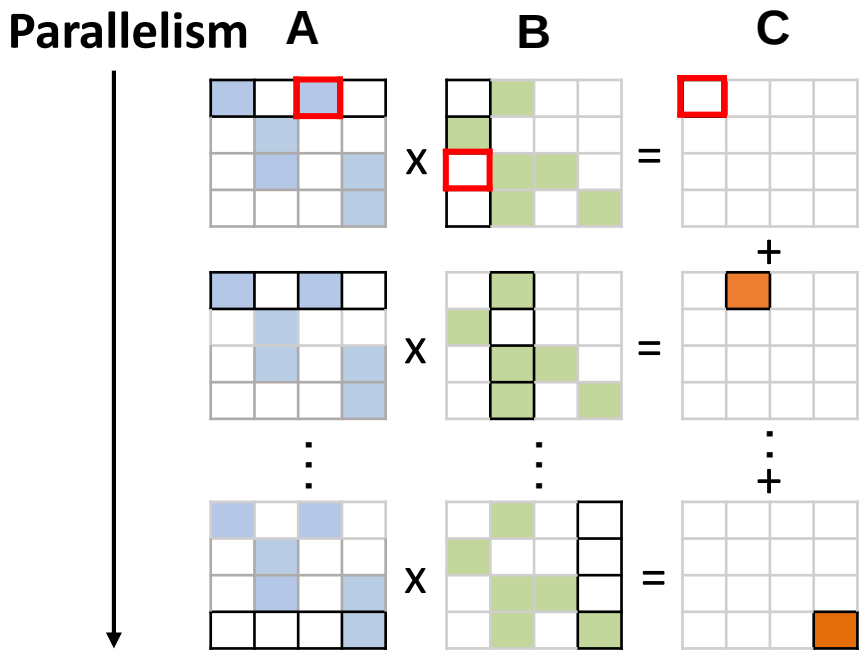

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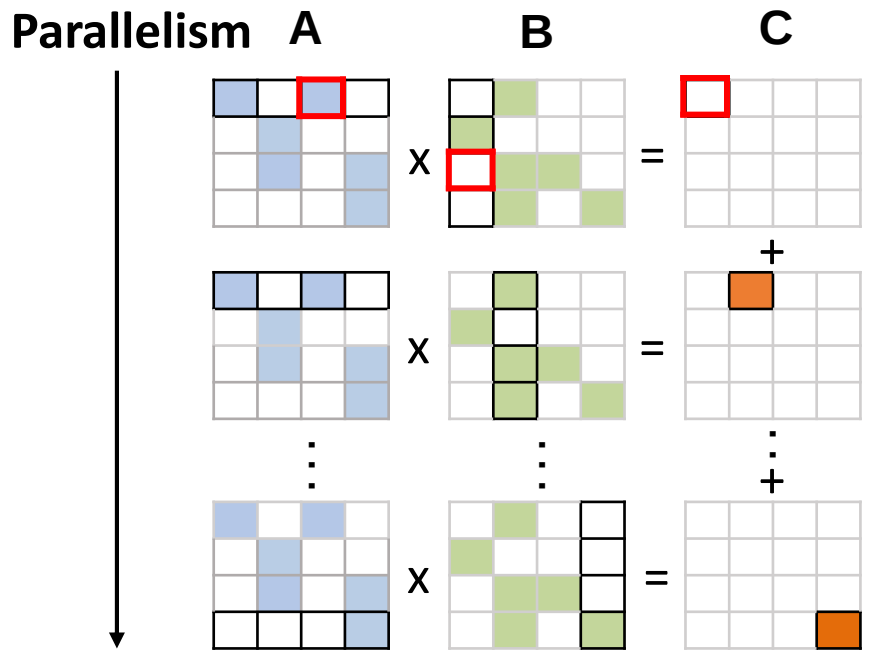

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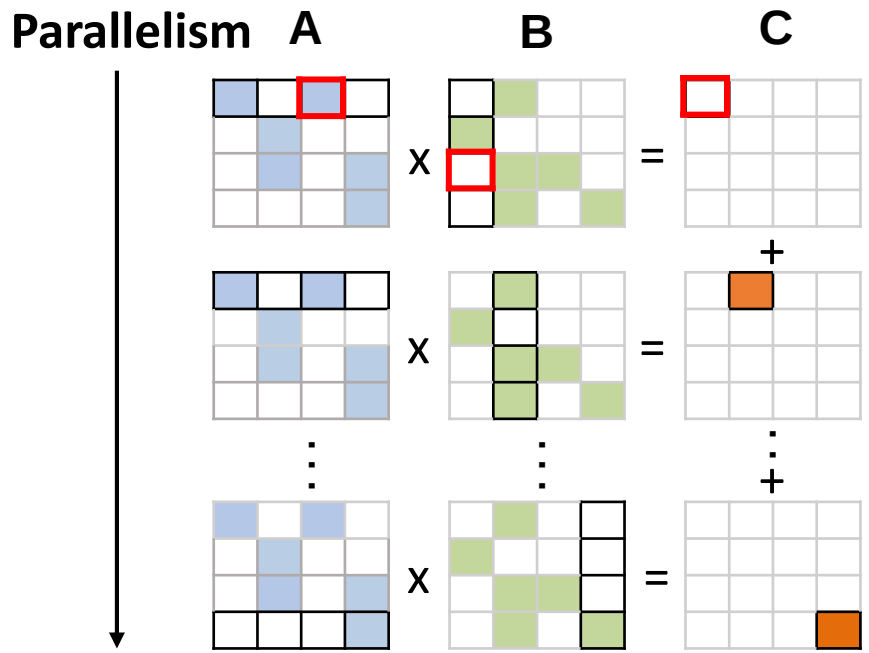

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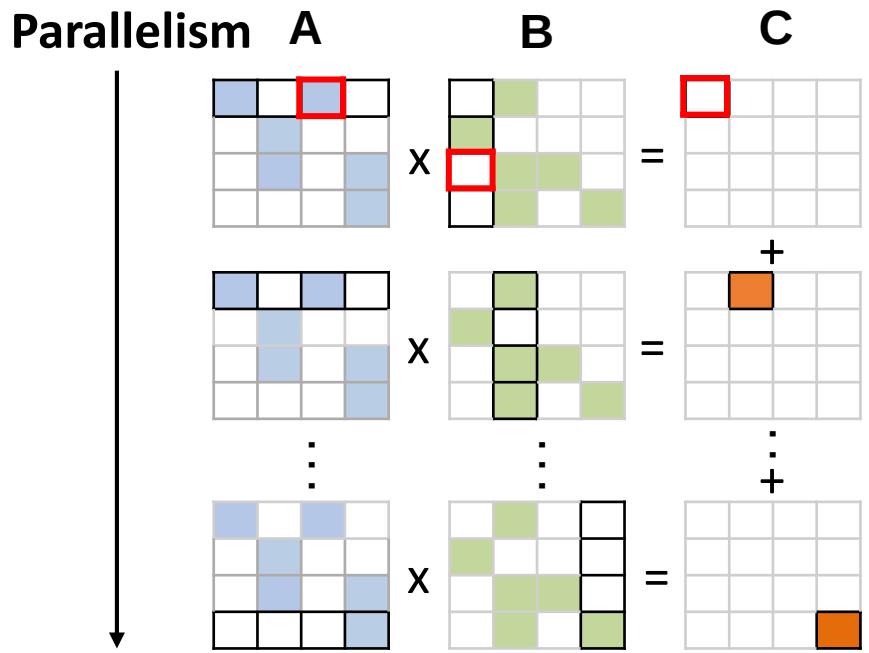

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Low on-chip memory requirements

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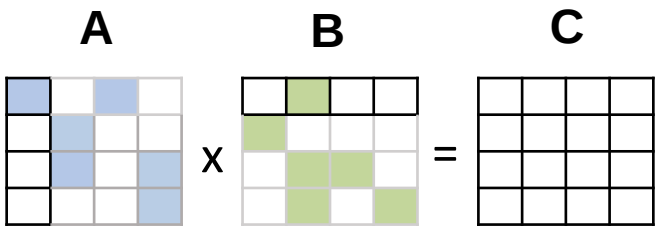

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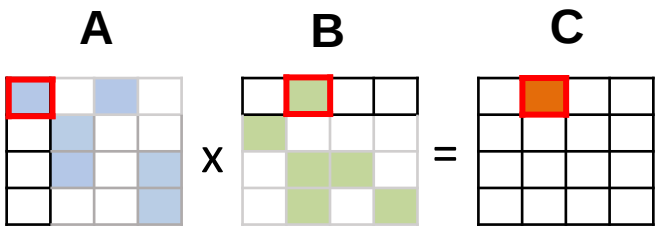

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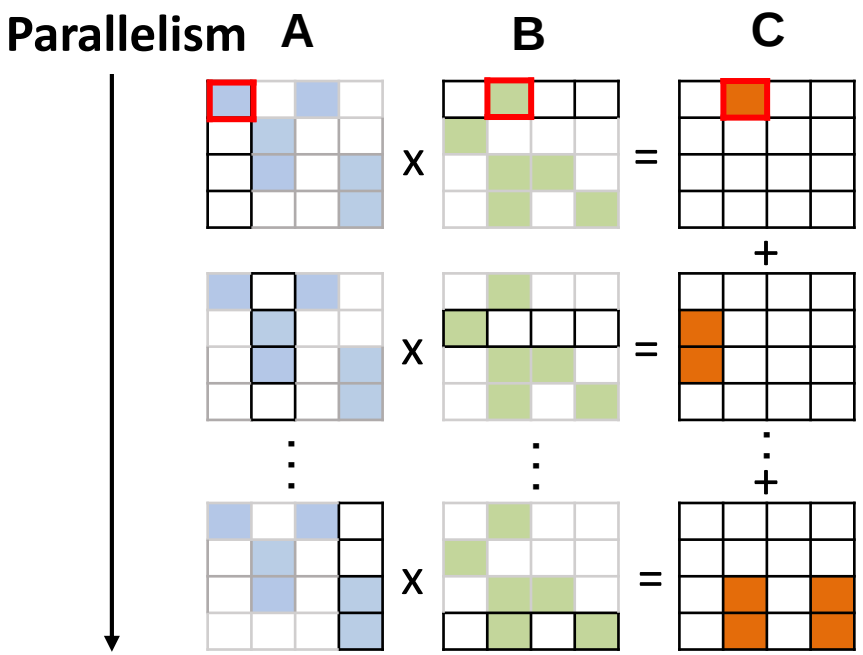

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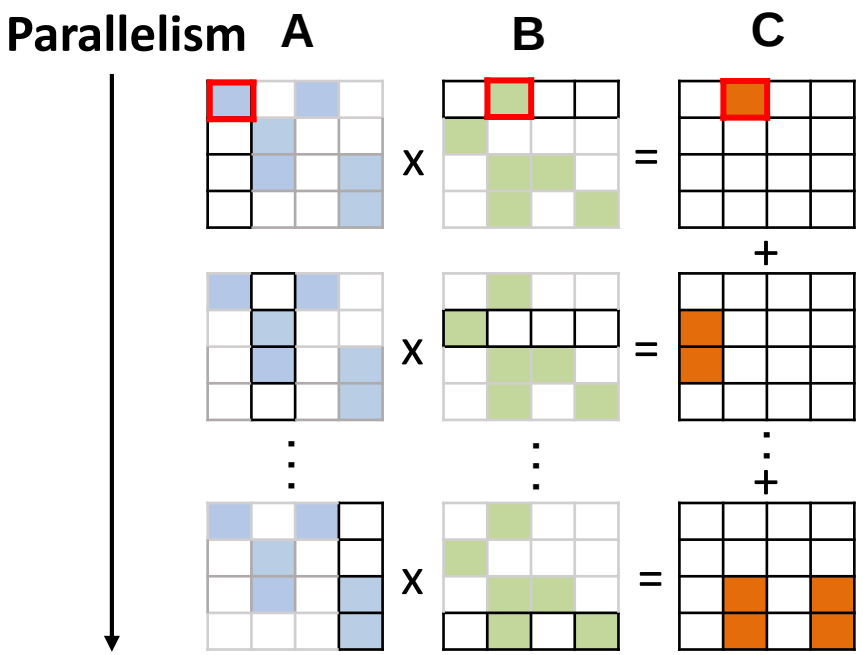

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Column-major format for A and row-major for B

Improvement in index matching

Synchronization

High on-chip memory requirements

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Challenges with Sparse-Sparse MM Acceleration

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Challenges

- **Choice Of Algorithm**
  - Inner & outer product not efficient
- **Memory Bandwidth**
  - Low data reuse
- **Sparse Output Matrix**
  - Position of non-zeros are unknown
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Solution

- **MatRaptor:** An efficient hardware accelerator for sparse-sparse MM
- **Key Idea:** Co-design **algorithm** and **sparse format**

Proposed Approach: Row-wise Product

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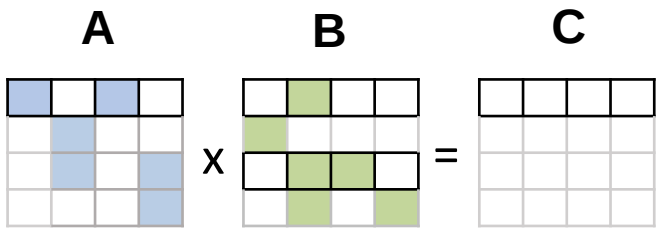

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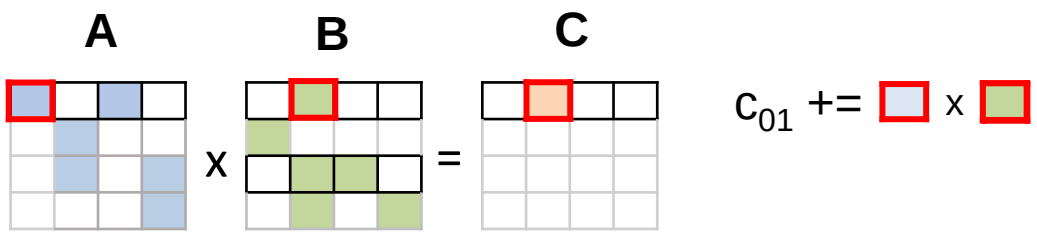

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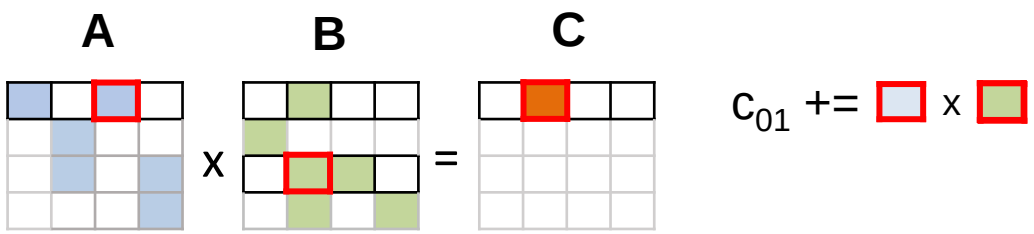

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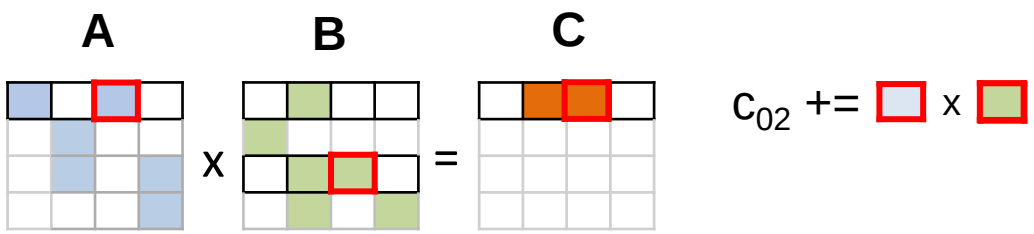

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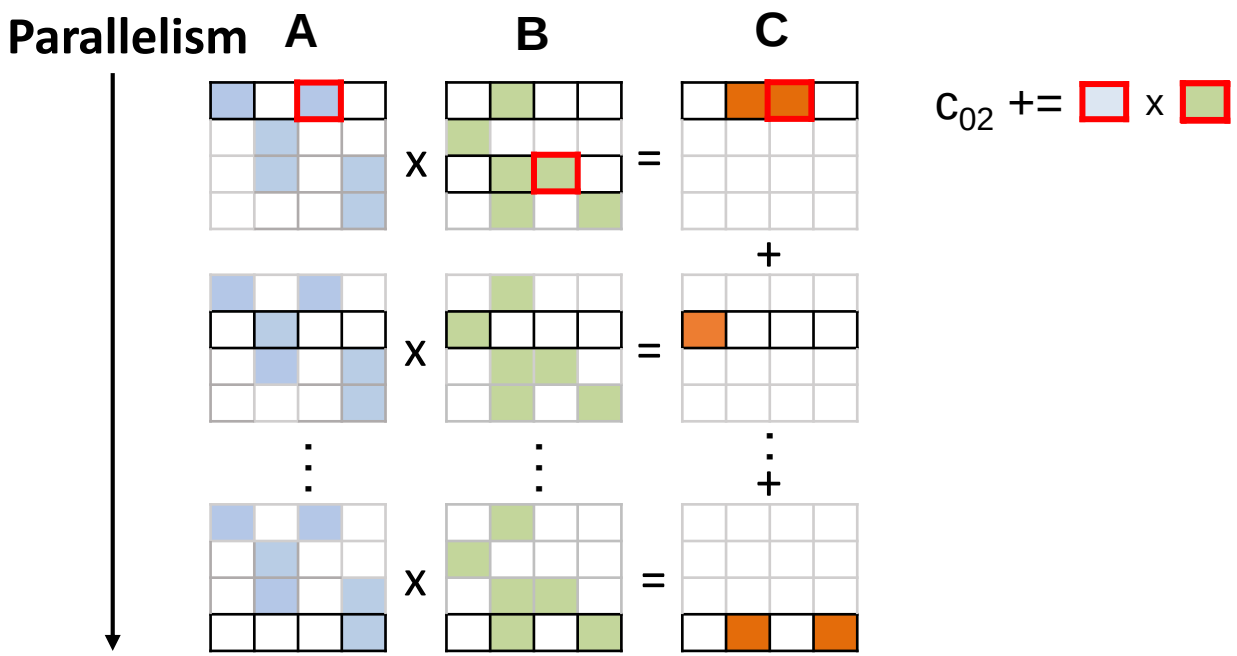

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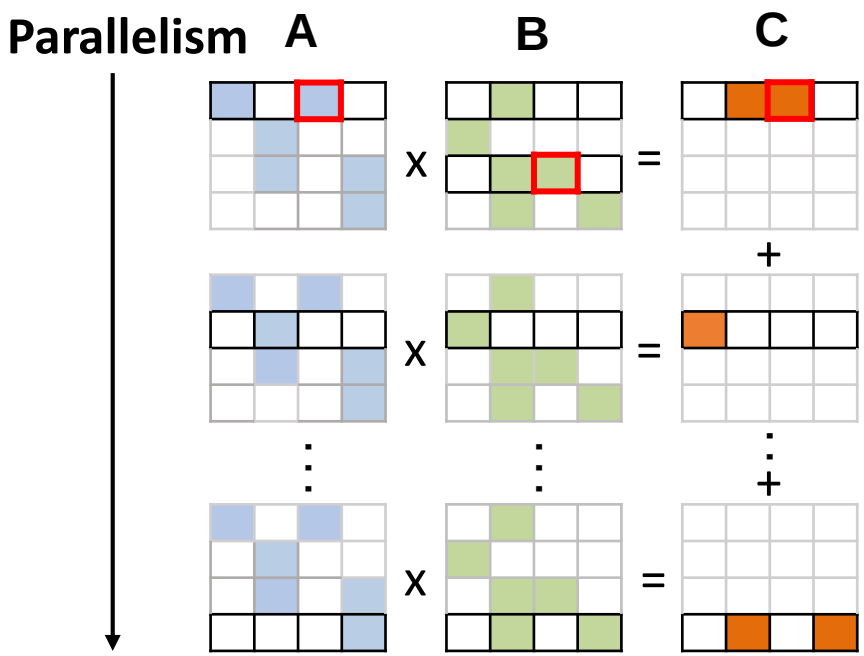

c_{02} += x

Consistent formatting

Row-major format for A, B and C

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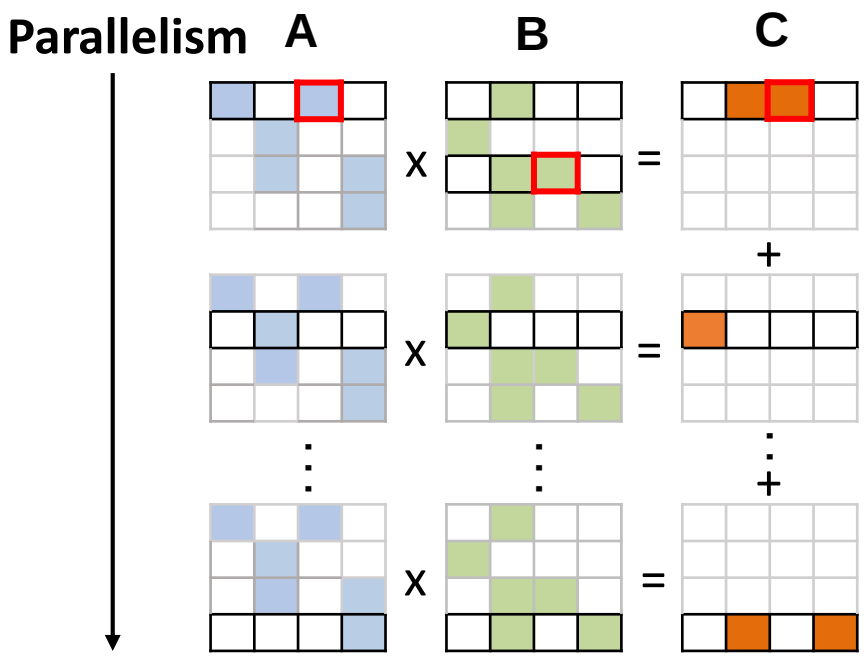

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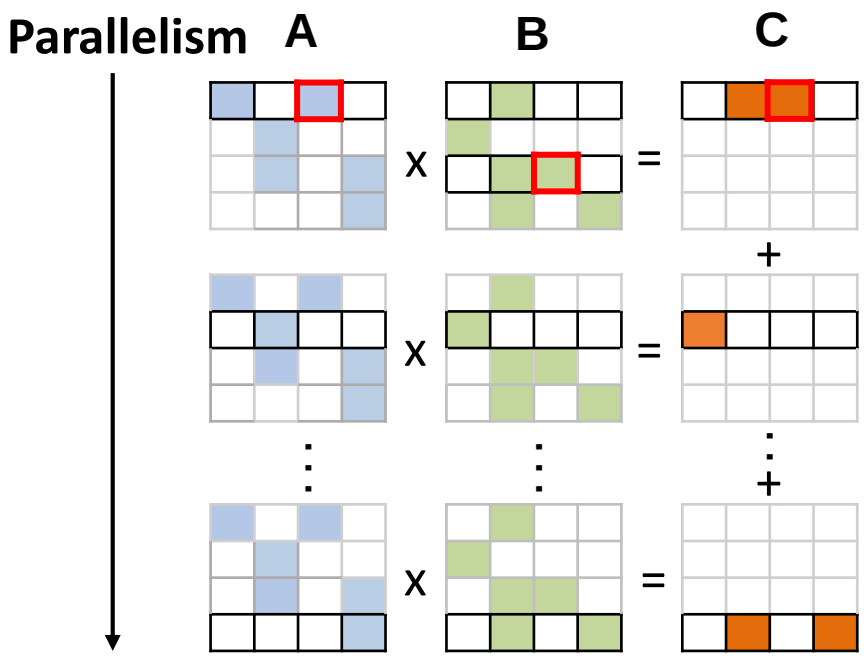

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No synchronization

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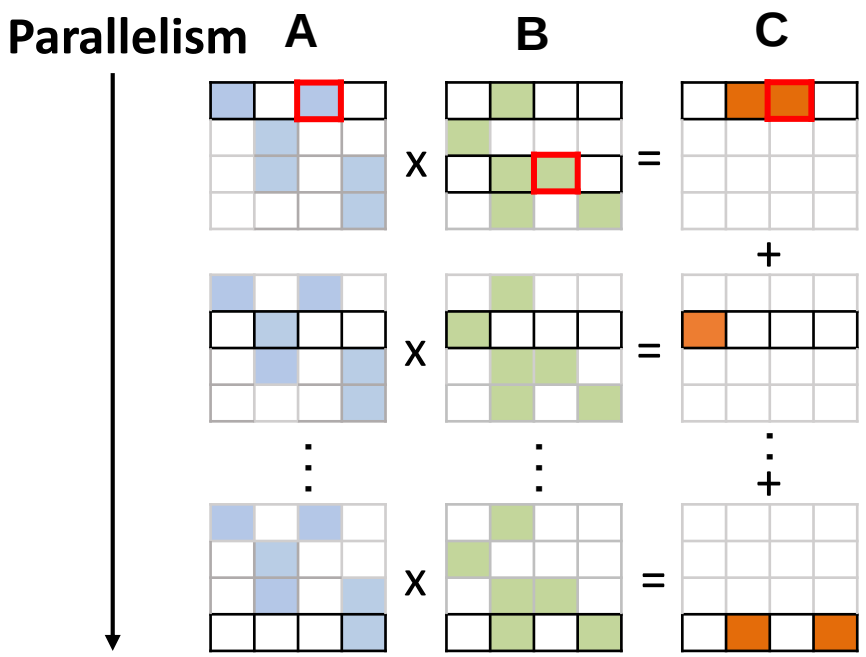

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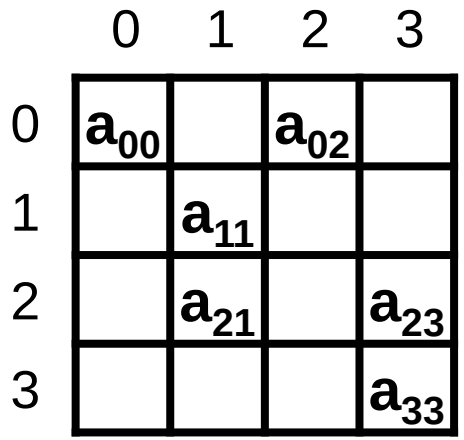
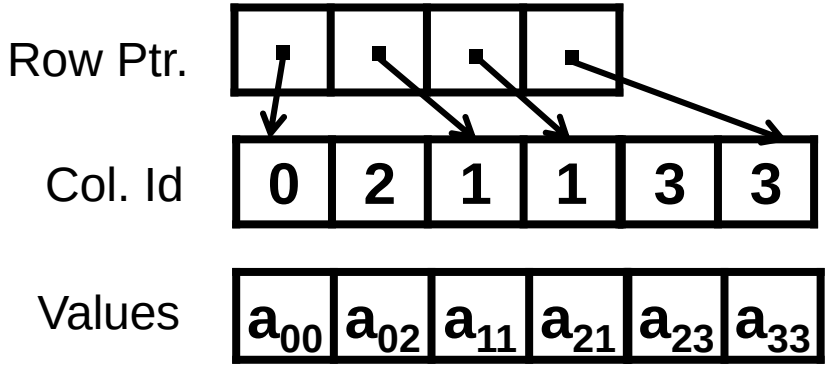
Medium/low on-chip memory requirements

CSR for Sparse-Sparse MM



Compressed Sparse Row (CSR)



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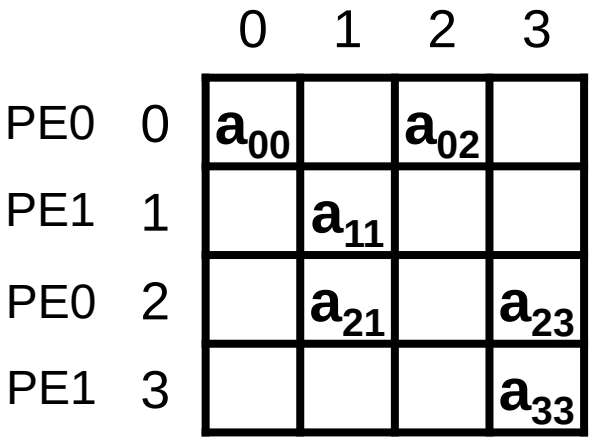

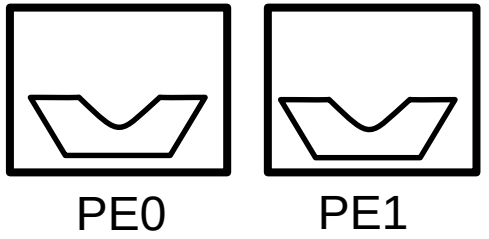

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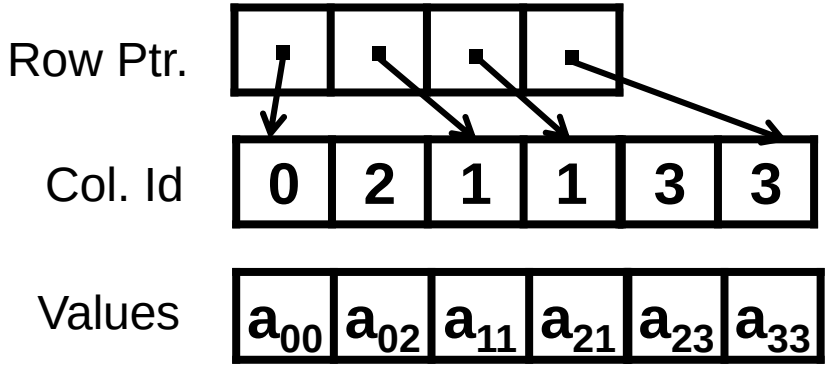
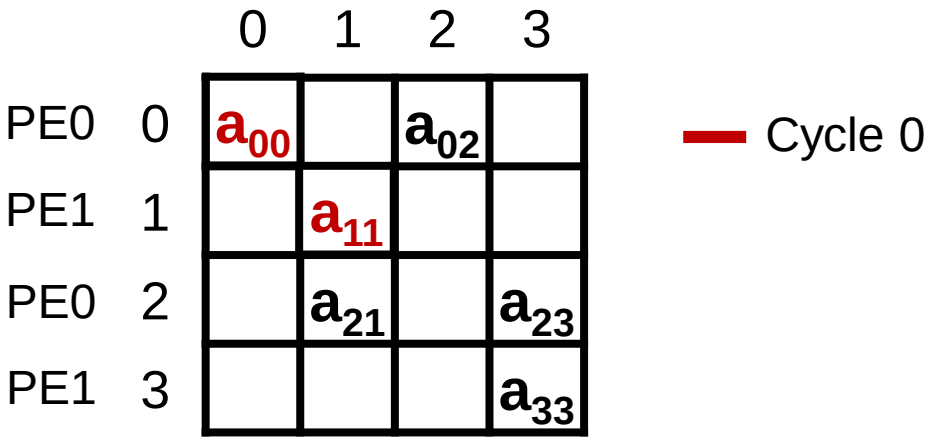
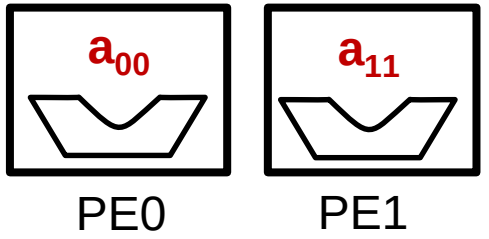
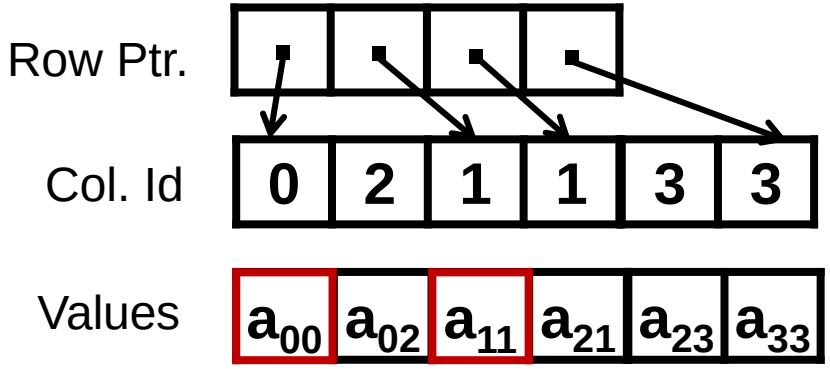


CSR for Sparse-Sparse MM

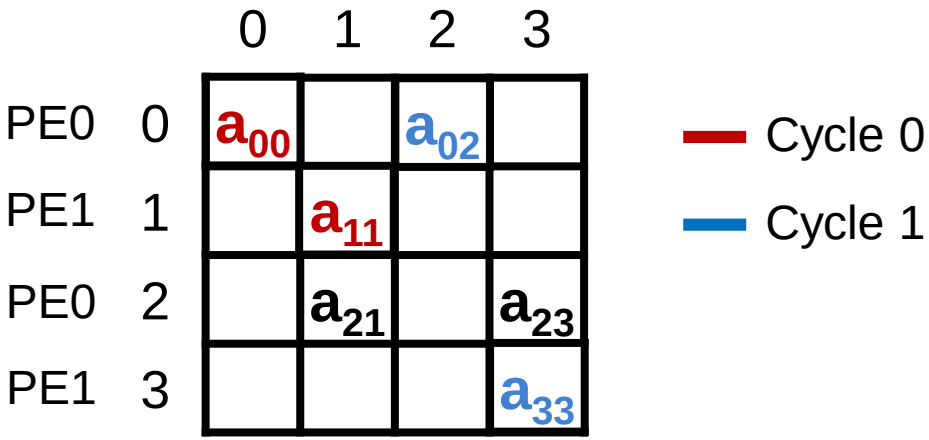


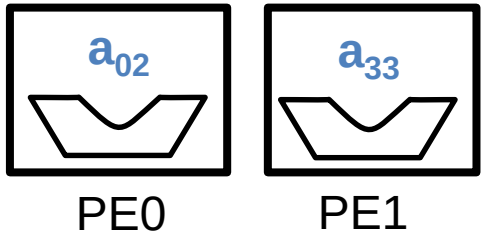


Compressed Sparse Row (CSR)



CSR for Sparse-Sparse MM





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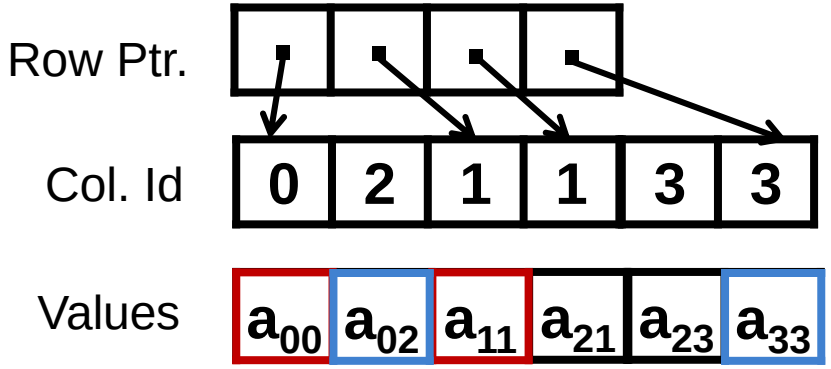

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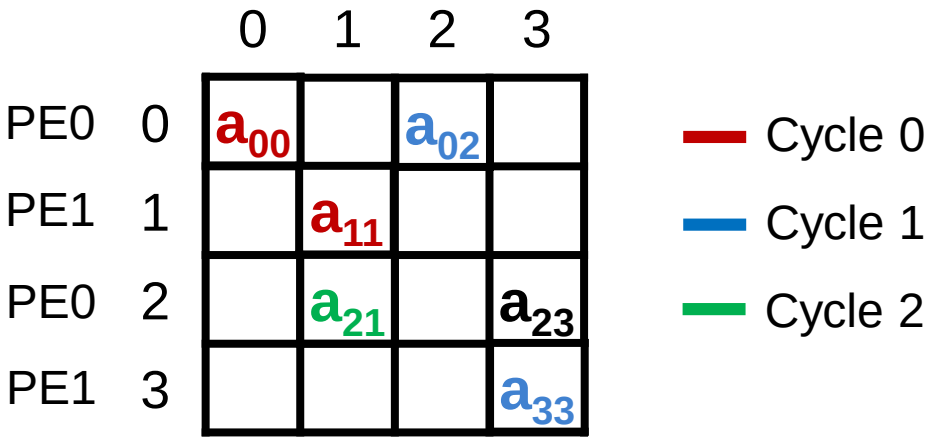

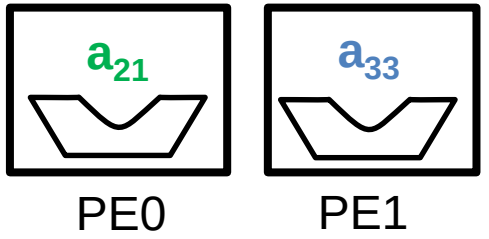

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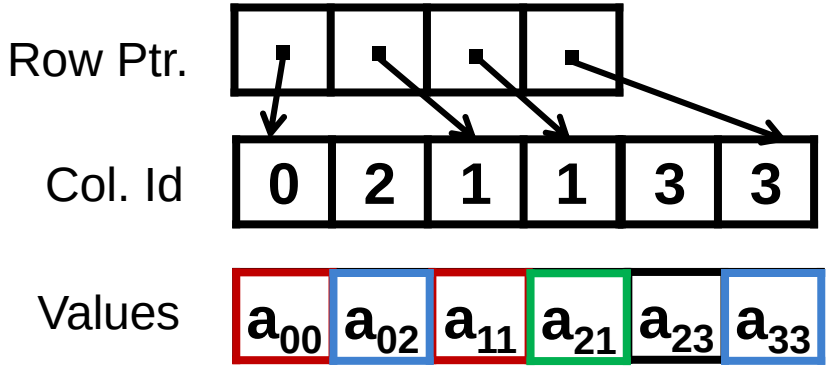

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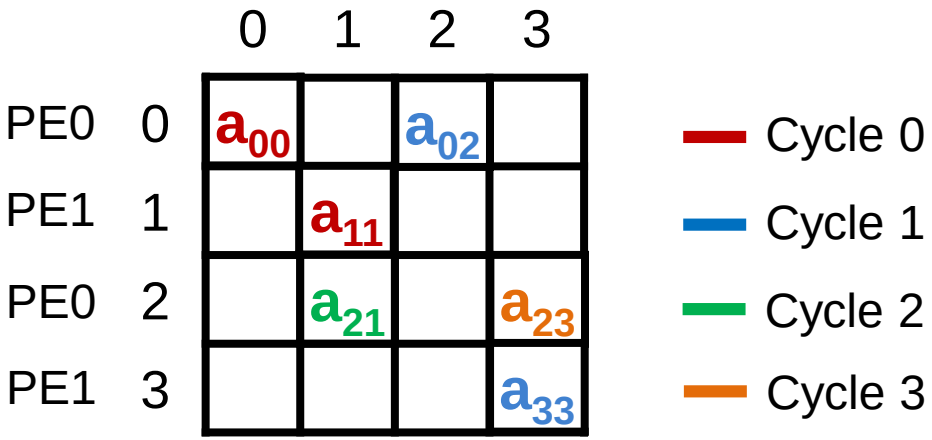

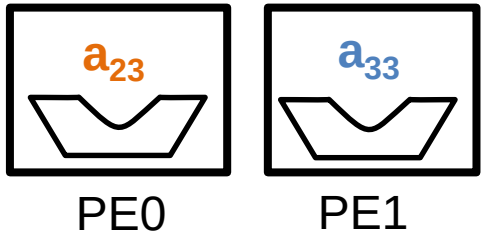

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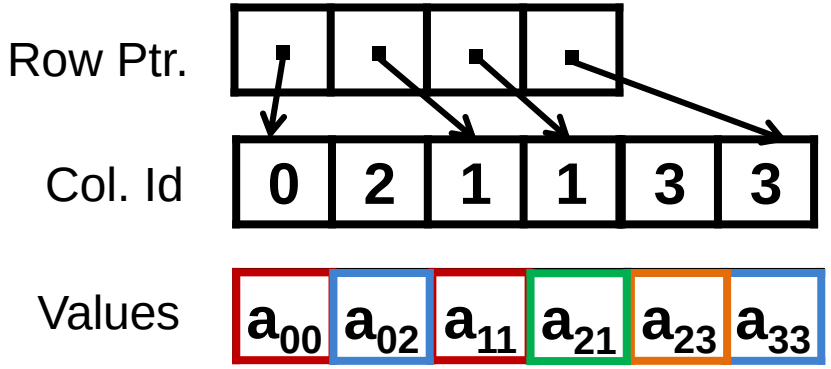
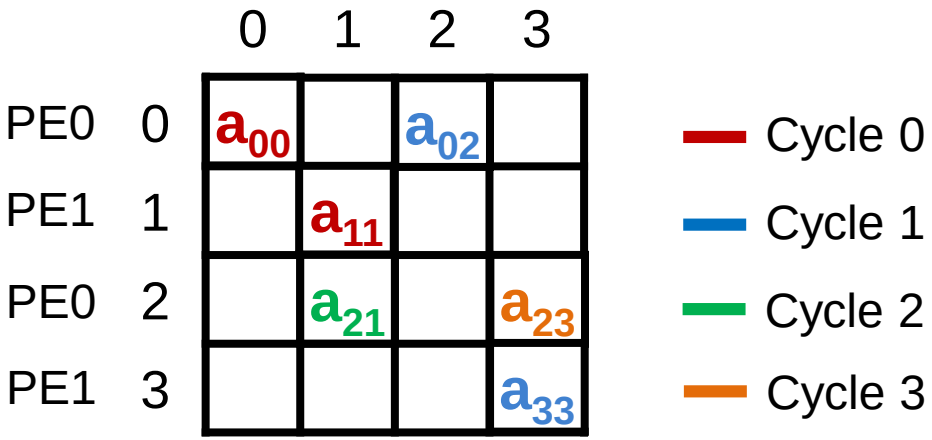
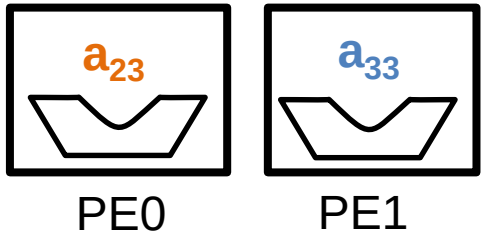


CSR for Sparse-Sparse MM





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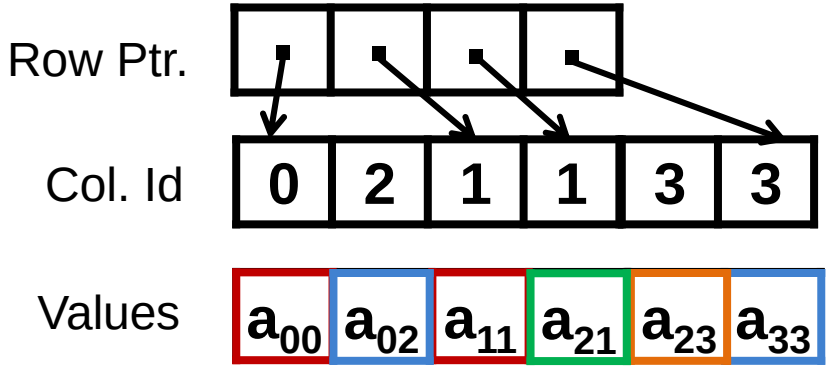

Non-Streaming accesses

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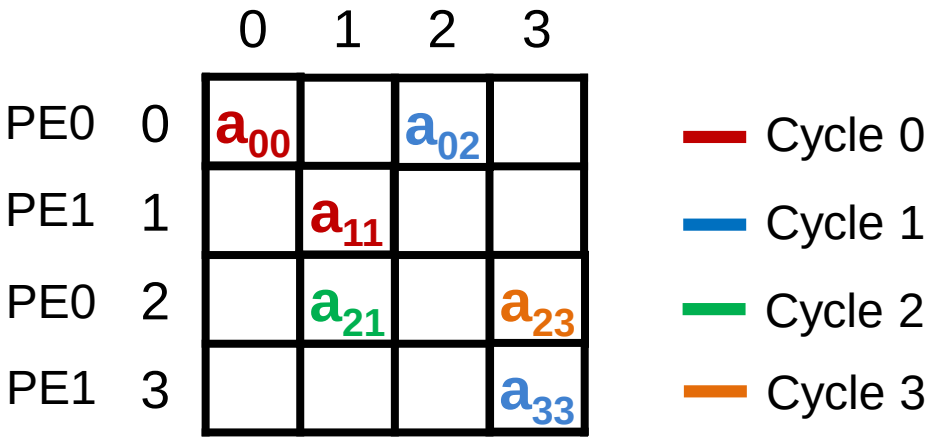
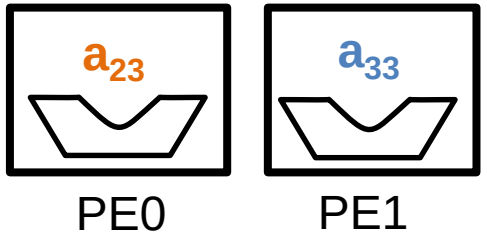
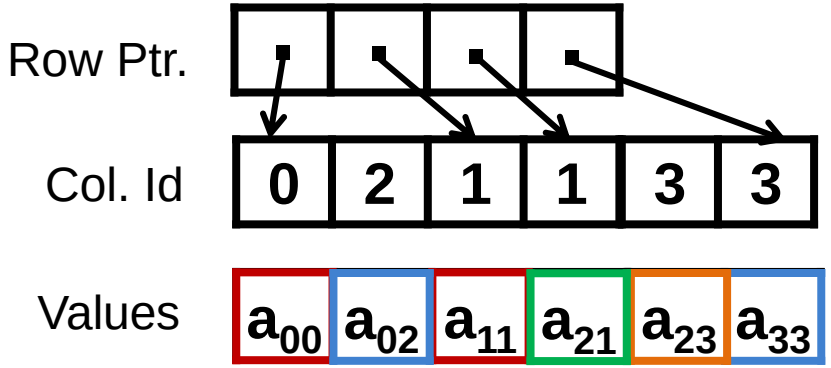




Compressed Sparse Row (CSR)



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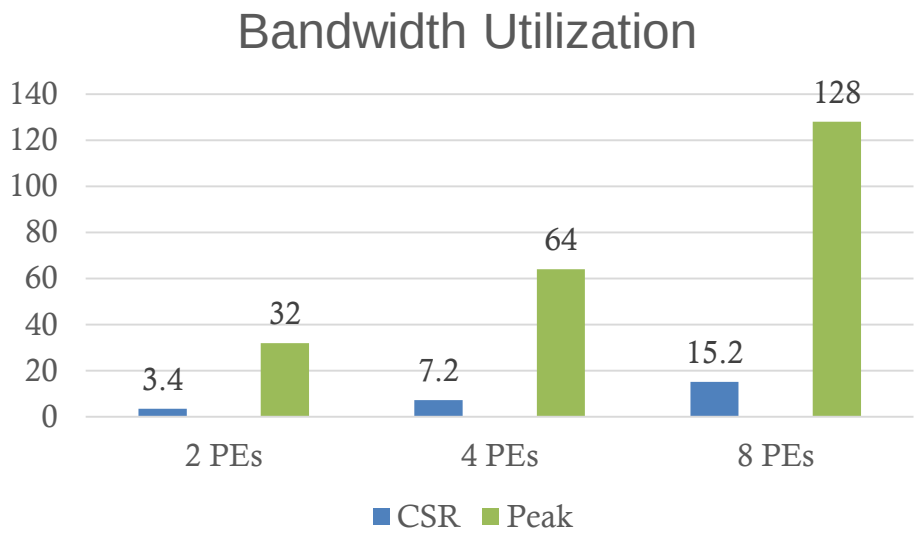
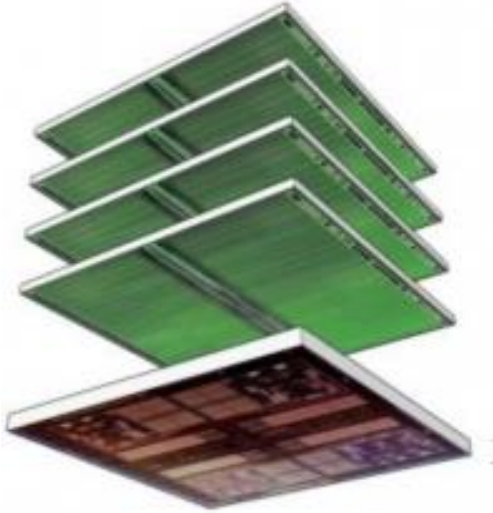


High Memory Bandwidth with HBM

High Memory Bandwidth with HBM

- **HBM can provide upto 128 GB/s**

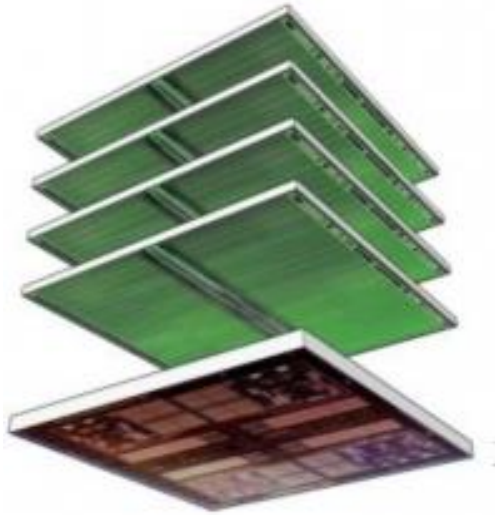


HBM with 8 pseudo-channels
(4 physical channels)

High Memory Bandwidth with HBM

- **HBM can provide upto 128 GB/s**

- **Memory-Level Parallelism**
  - **Can be achieved by accessing in parallel**
    - **Memory channels**
    - **Memory banks**
  - **Is hampered by**
    - **Channel conflicts**
    - **Bank conflicts**



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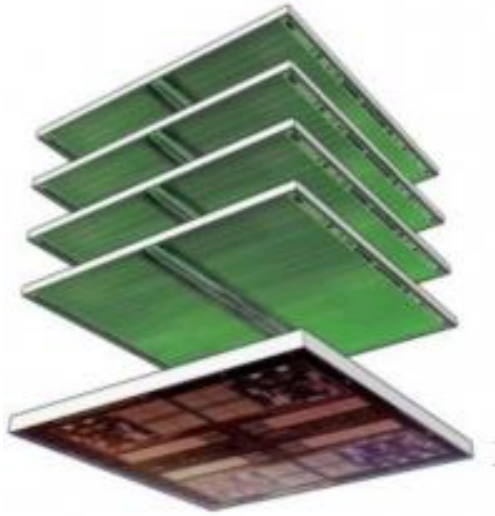

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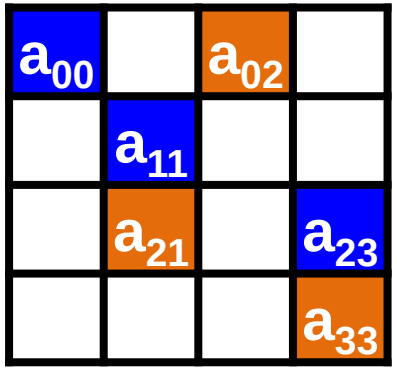
CSR



Assuming parallel row access
w/ two HBM channels

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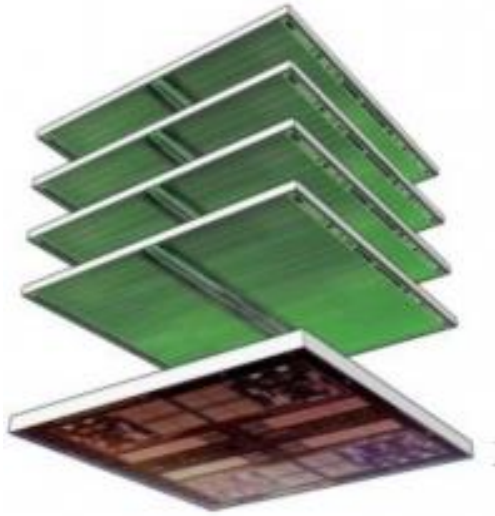
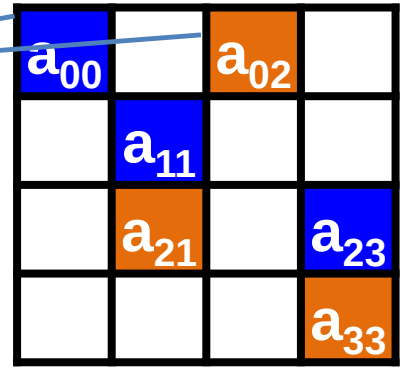


HBM with 8 pseudo-channels
(4 physical channels)

CSR

- **Single row split across channels**



Assuming parallel row access
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High Memory Bandwidth with HBM

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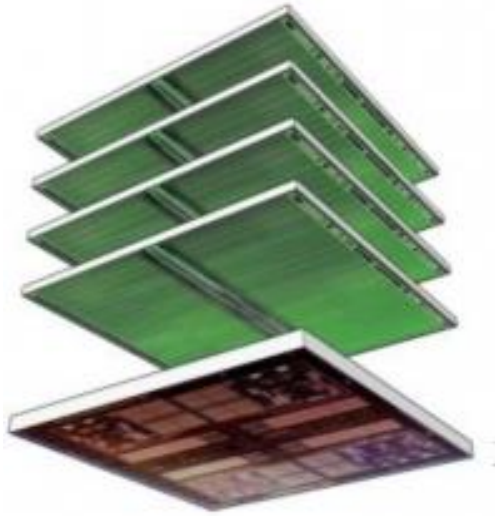
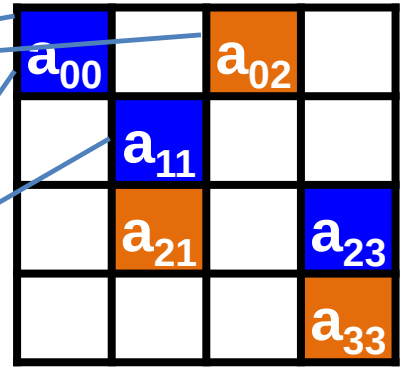


HBM with 8 pseudo-channels
(4 physical channels)

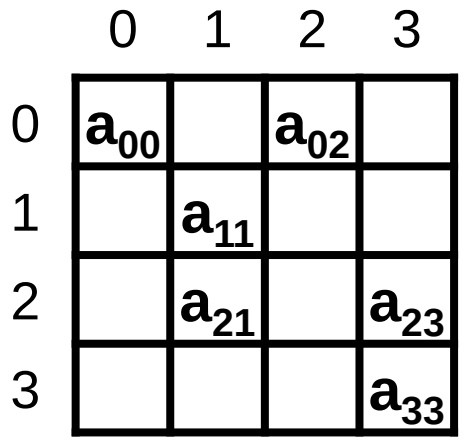
CSR

- **Single row split across channels**
- **Row parallelization incurs channel conflicts**

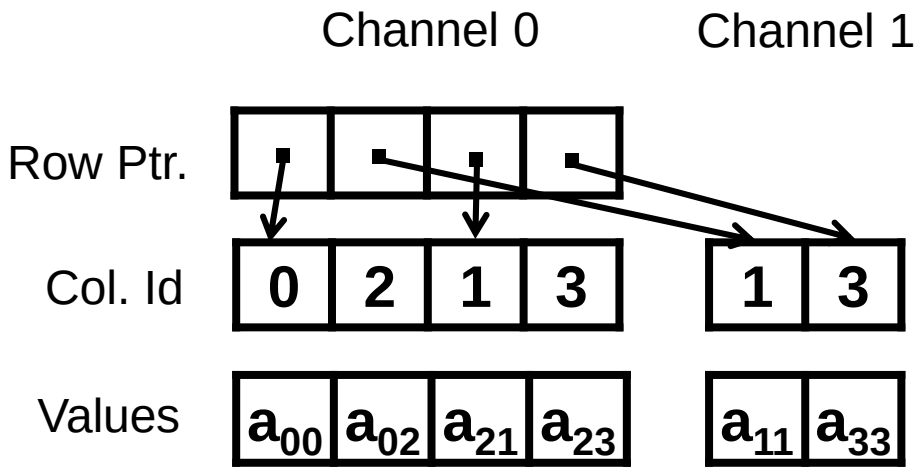


Assuming parallel row access
w/ two HBM channels

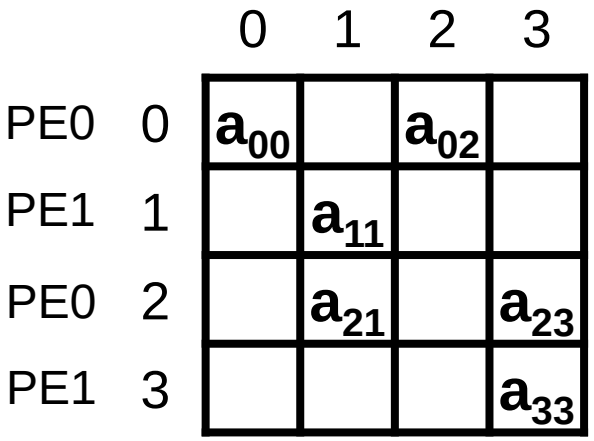
C²SR for Sparse-Sparse MM

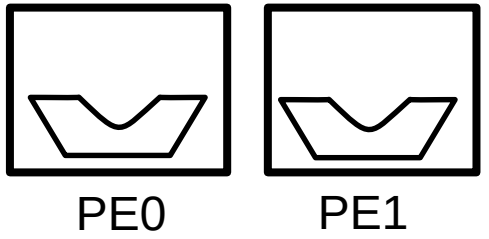


Cyclic Channel Sparse Row (C²SR)

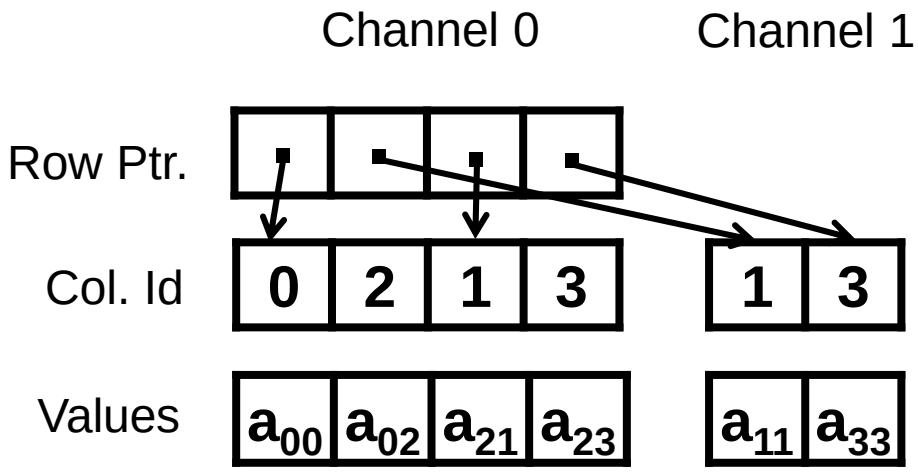


C²SR for Sparse-Sparse MM

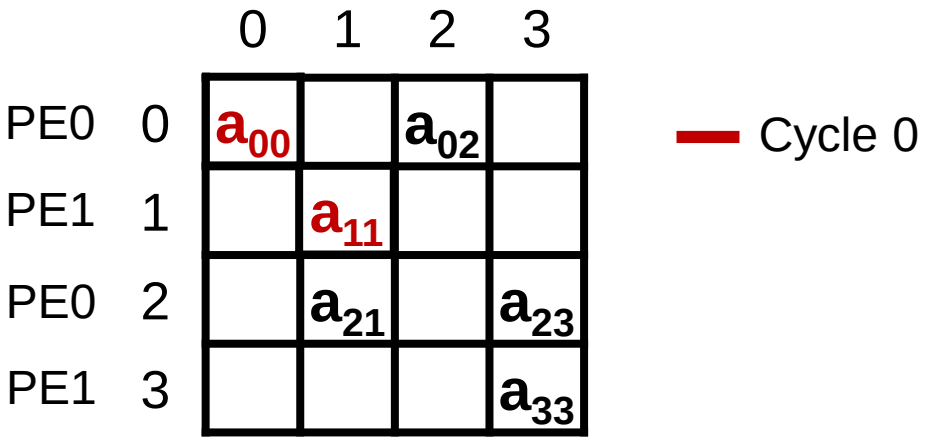


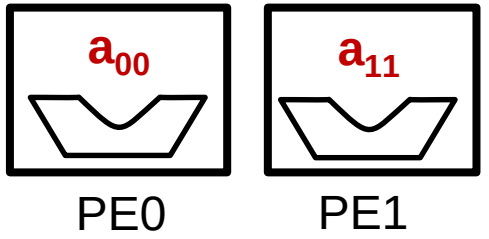


Cyclic Channel Sparse Row (C²SR)



C²SR for Sparse-Sparse MM





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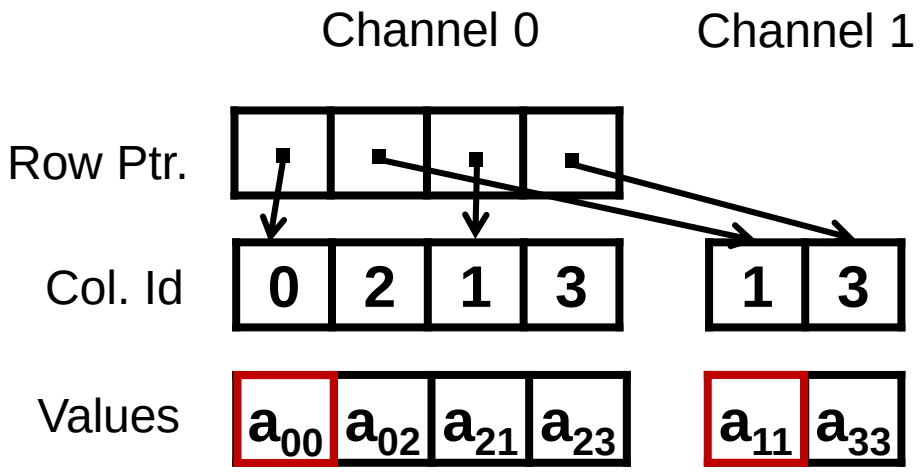
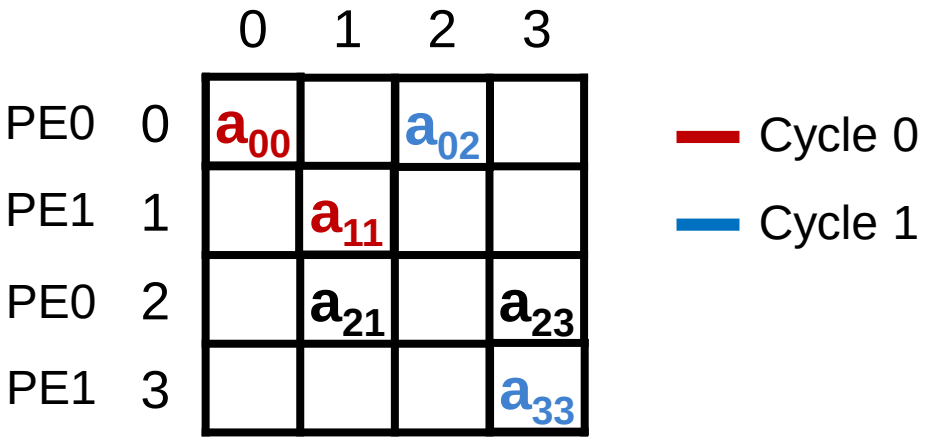
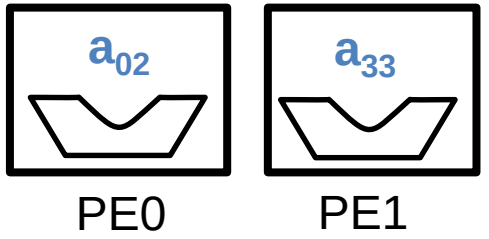


C²SR for Sparse-Sparse MM





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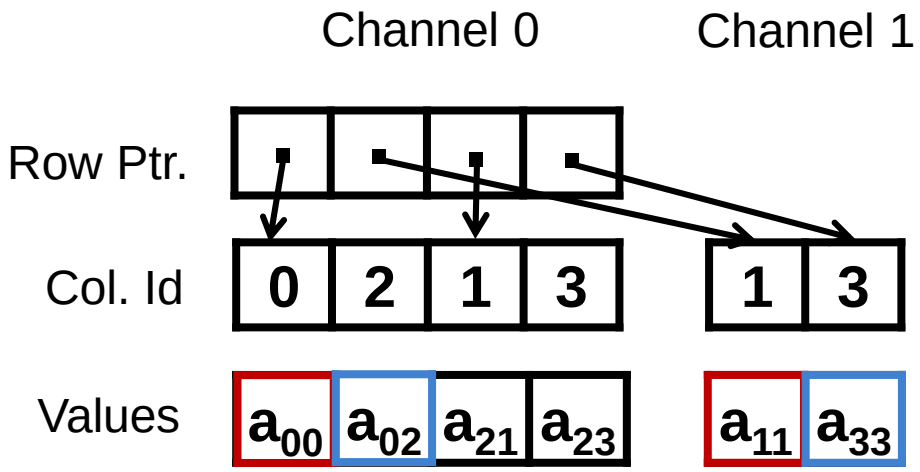

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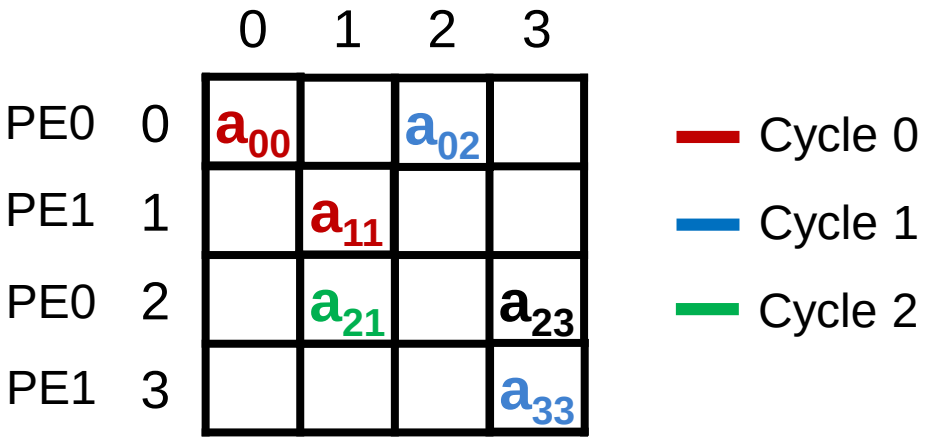

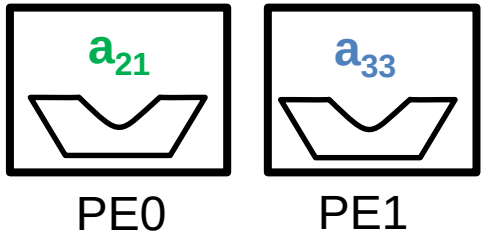

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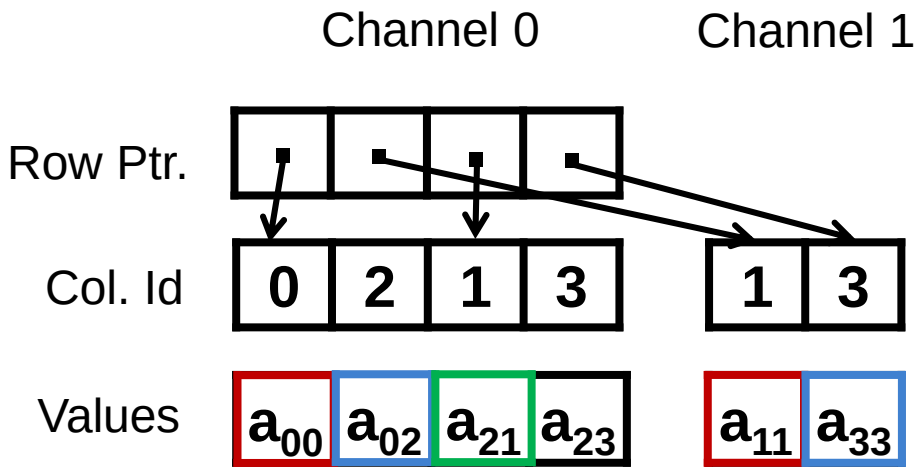

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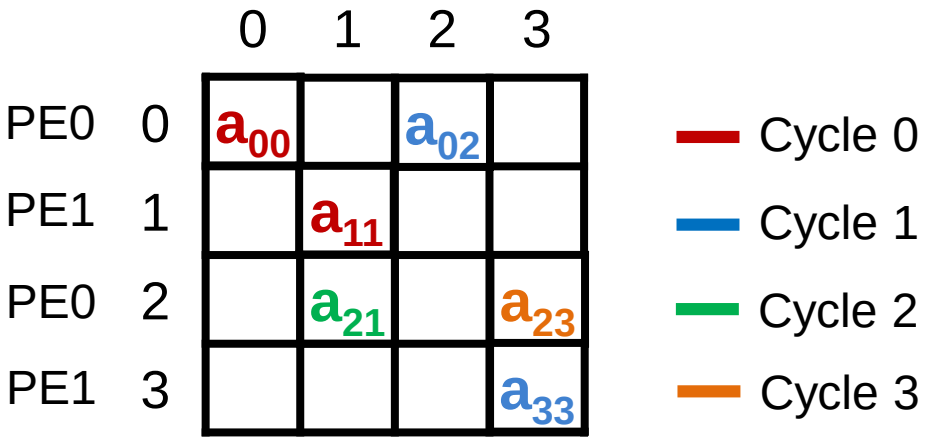

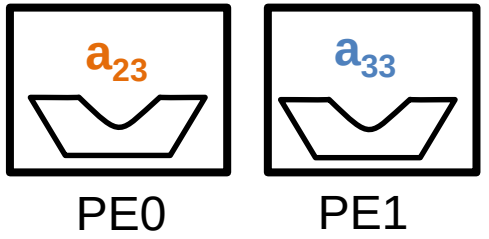

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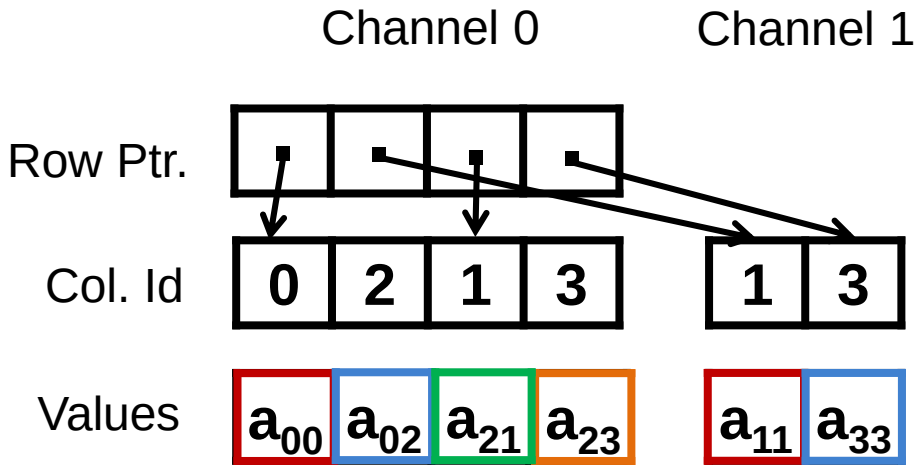

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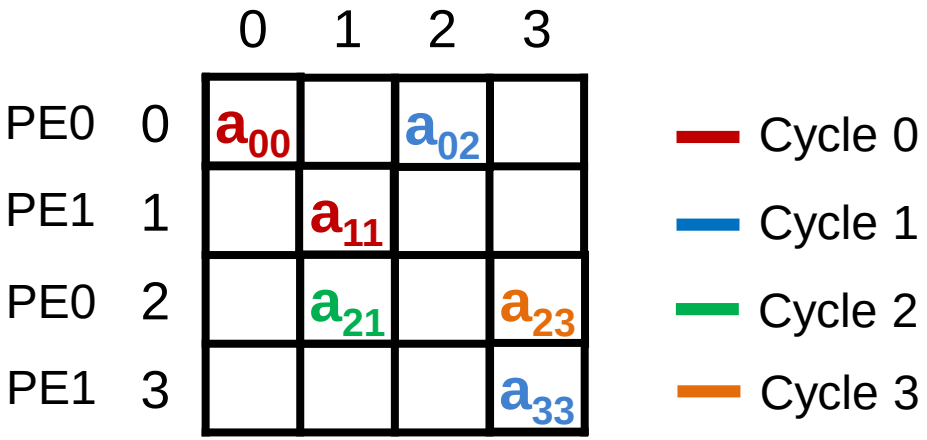

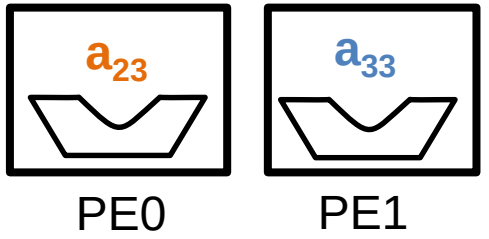

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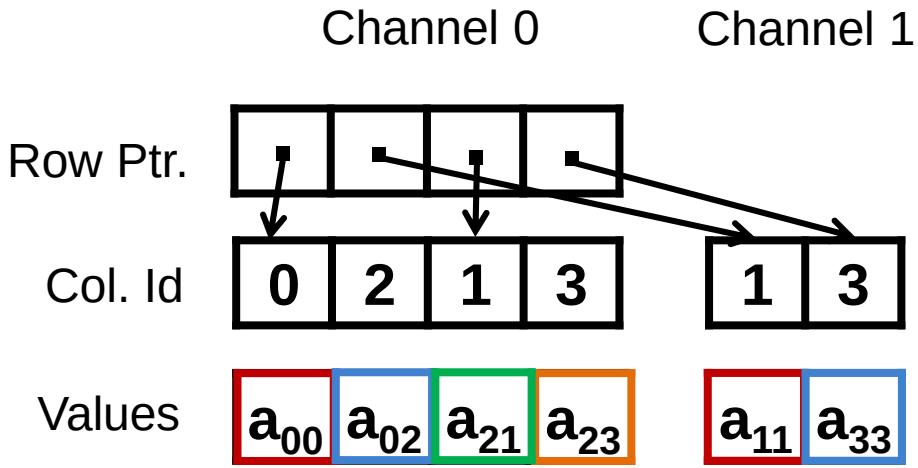
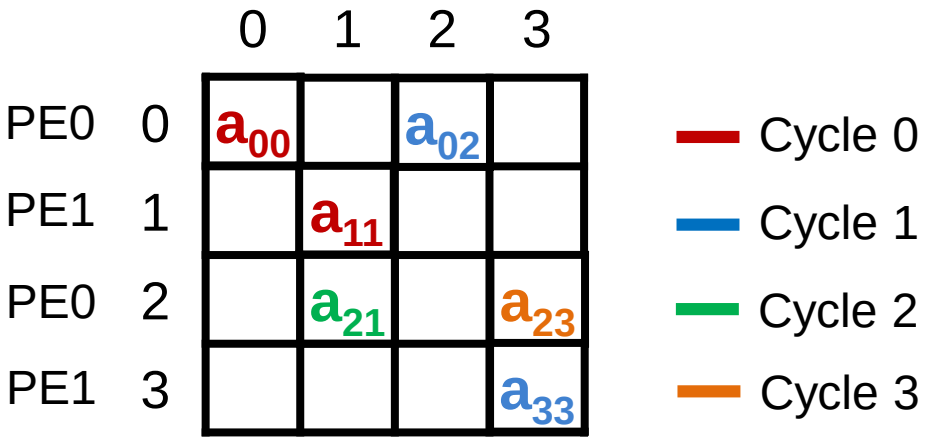


Streaming accesses in each channel

C²SR for Sparse-Sparse MM



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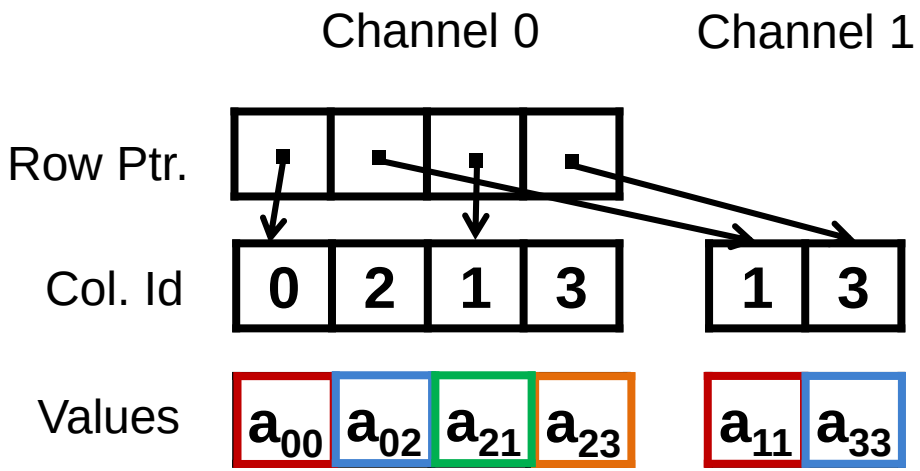

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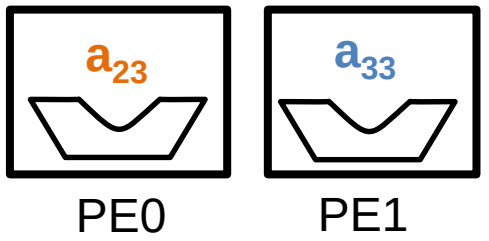
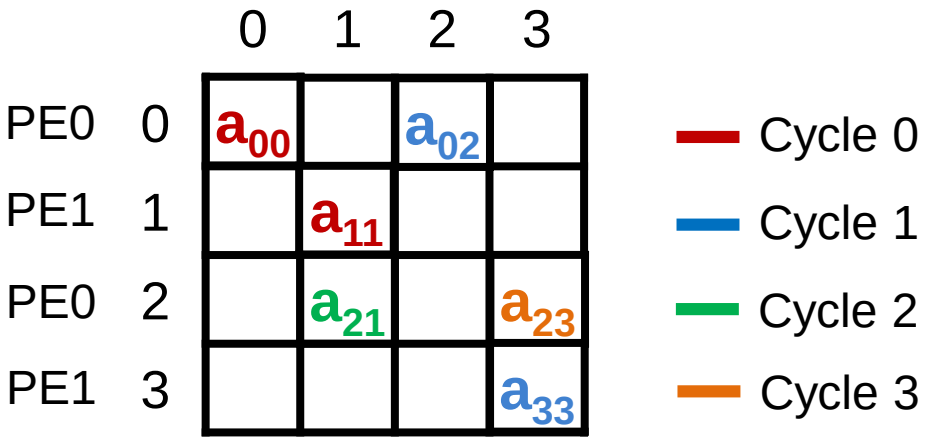


C²SR

- **None of the row split across channels**
- **Row parallelization does not incur channel conflicts**

C²SR for Sparse-Sparse MM



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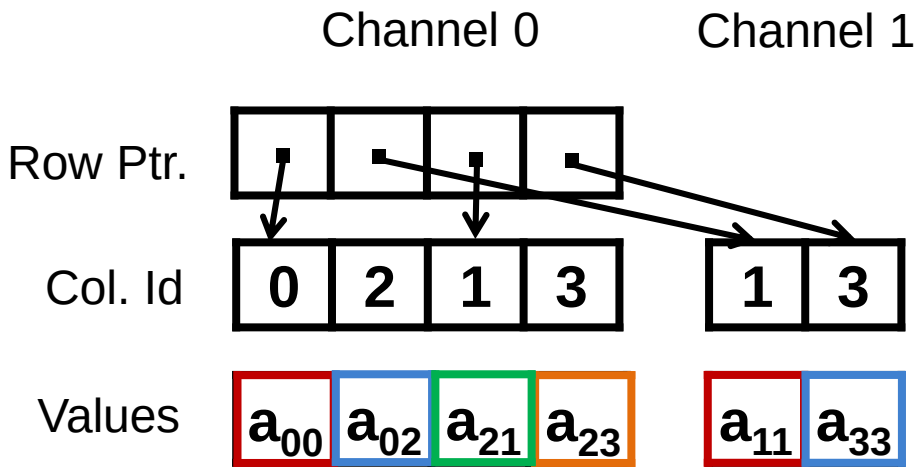

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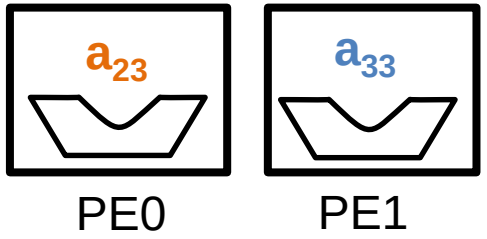
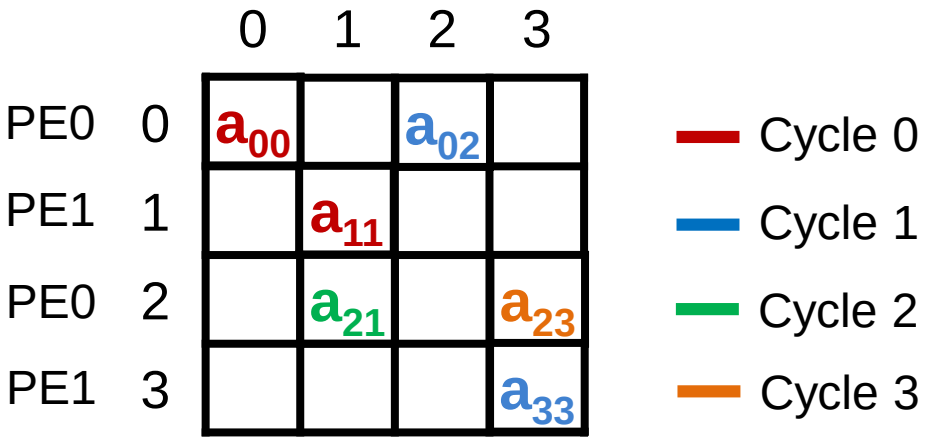
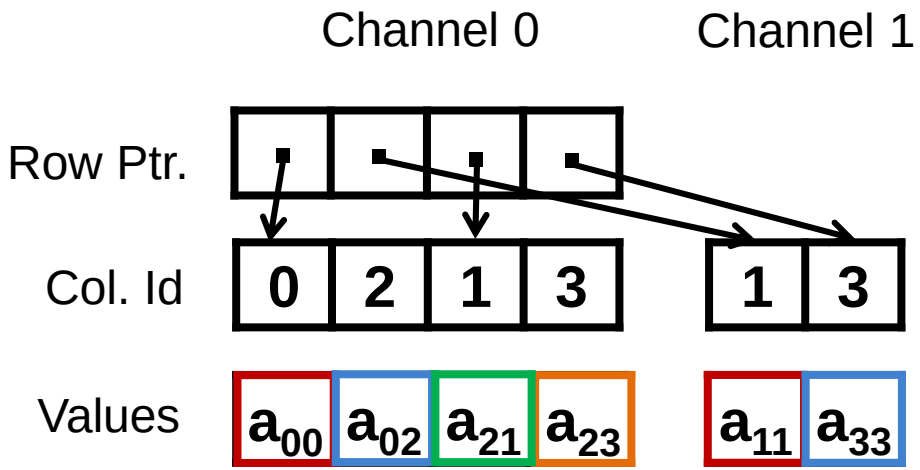


Producing the output matrix in C²SR format means different PEs can work independently

C²SR for Sparse-Sparse MM



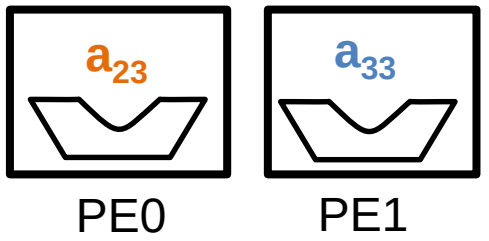
Cyclic Channel Sparse Row (C²SR)



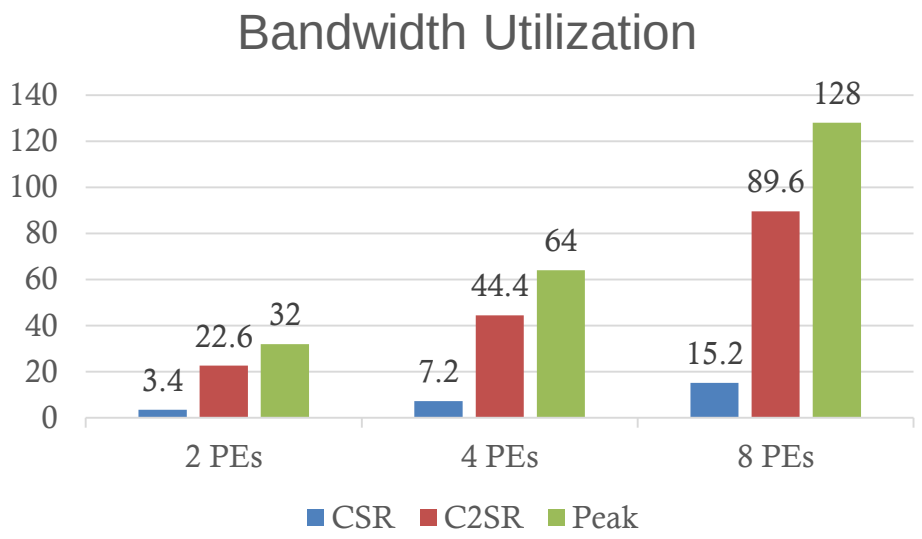
Streaming accesses in each channel

C²SR

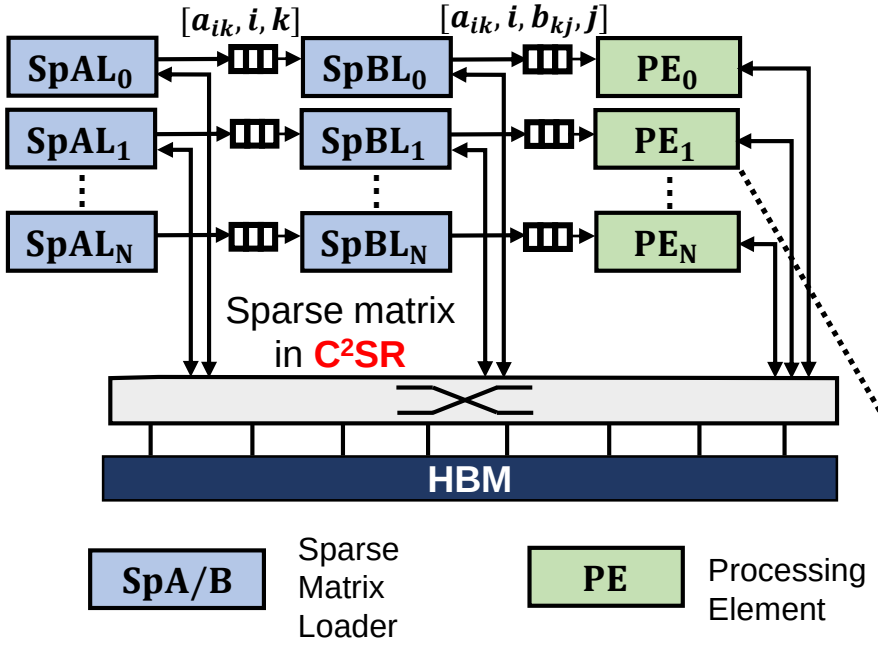
- **None of the row split across channels**
- **Row parallelization does not incur channel conflicts**



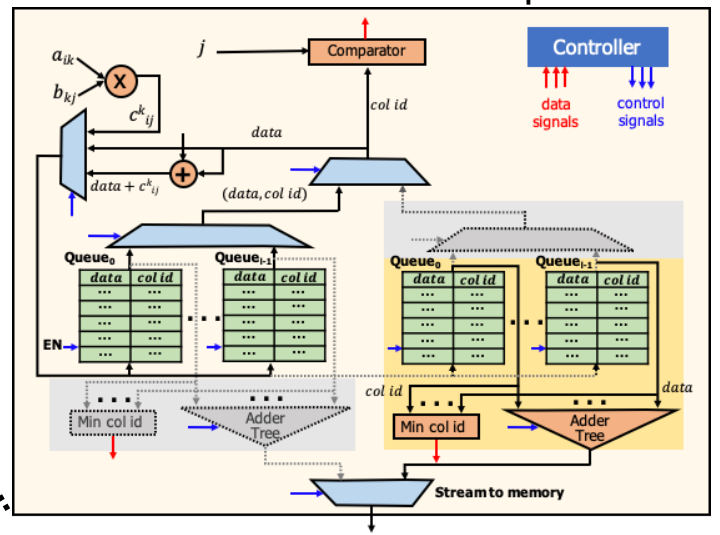
Producing the output matrix in C²SR format means different PEs can work independently

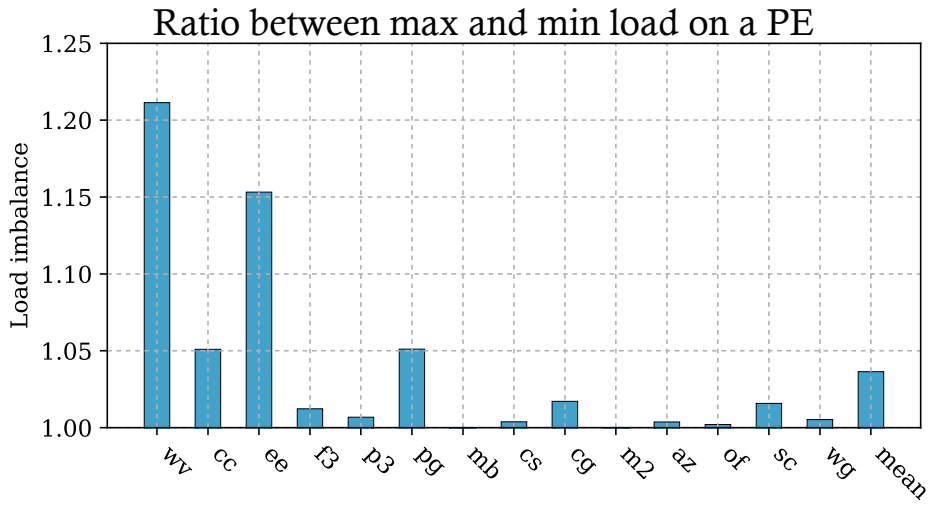


MatRaptor Architecture



Each PE handles one output row





- **Reads/writes in C²SR format** to exploit HBM bandwidth
- **Two-level load balancing** for high compute utilization
  - Round-robin execution across PEs
  - Decoupled access, multiply & merge for each PE

Work among PEs are mostly well balanced

Evaluation Methodology

- **Cycle-level simulation in gem5**
  - 8 PE array, Memory Width 128 bytes
  - 10 4 KB Queues (RAMs) per PE
  - HBM: 8 128-bit channels (128 GB/s peak bandwidth)

- **RTL Modeling of a PE using PyMTL**

- **Baselines**
  - CPU: Intel(R) Xeon(R) CPU E7-8867
    - Intel MKL
  - GPU: Titan XP
    - CuSparse
  - Accelerator:
    - OuterSPACE[5]

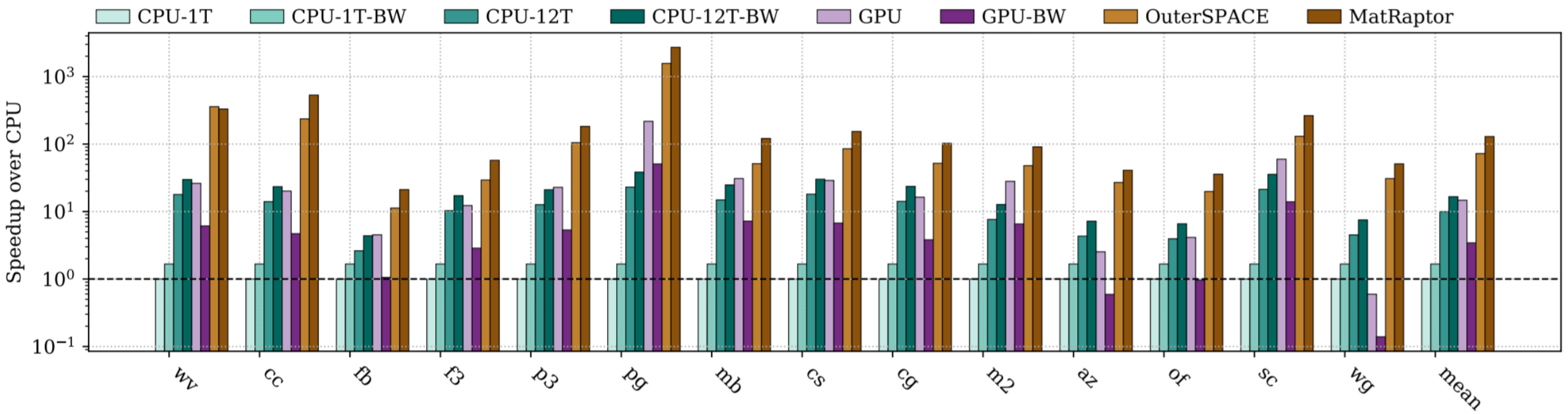
- **Datasets**
  - SuiteSparse[6]

Area and Power Breakdown

Component	Area (mm^2)	%	Power (mW)	%
PE	1.981	87.77 %	1050.57	78.11 %
– Logic	0.080	3.54 %	43.08	3.20 %
– Sorting Queues	1.901	84.22 %	1007.49	74.90 %
SpAL	0.129	5.71 %	144.15	10.71 %
SpBL	0.129	5.71 %	144.15	10.71 %
Crossbars	0.016	0.7 %	6.067	0.45 %
Total	2.257	100 %	1344.95	100 %

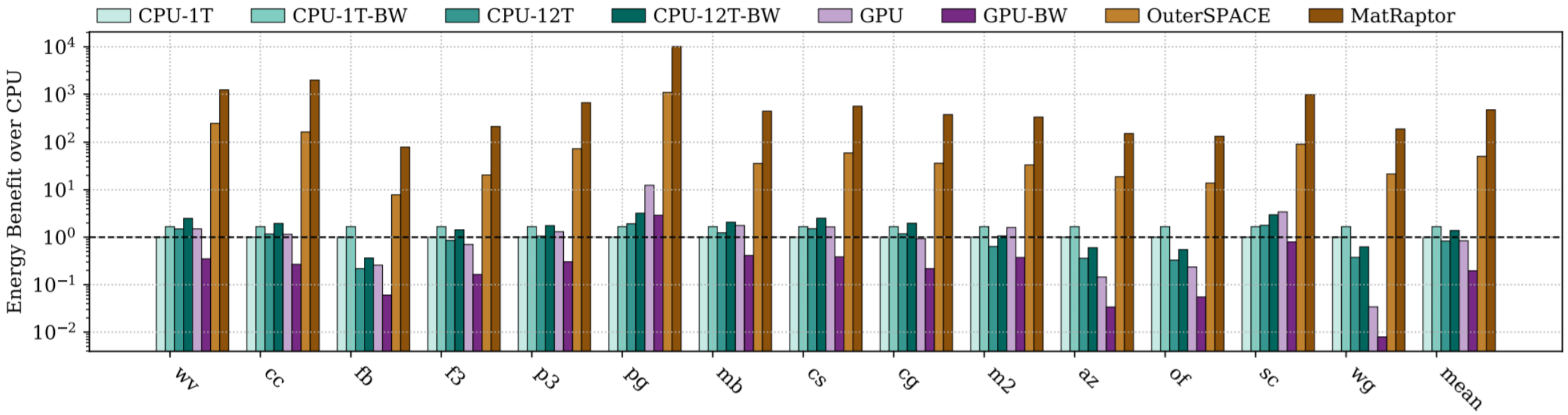
[5] Pal, Subhankar, et al. "Outerspace: An outer product based sparse matrix multiplication accelerator", Int'l Symp. on High Performance Computer Architecture (HPCA), 2018.
[6] T. A. Davis and Y. Hu, "The University of Florida sparse matrix collection," Trans. on Mathematical Software (TOMS), 2011

Speedup on Sparse-Sparse MM



MatRaptor is 129.2x, 7.9x and 1.8x faster than
CPU, GPU and OuterSPACE

Energy Efficiency on Sparse-Sparse MM



MatRaptor is 480x, 570x and 12x more energy-efficient than CPU, GPU and OuterSPACE

Conclusions & Future Work

- **MatRaptor, a new sparse-sparse MM accelerator, exploiting the co-design of hardware and sparse storage format**
  - First accelerator that uses row-wise product approach
  - A novel sparse storage format C^2SR to achieve high-memory bandwidth
  - Significant speedup and energy efficiency over CPU, GPU, and OuterSPACE

- **Future Work**
  - Integrate MatRaptor into a many-tiny-core system
  - Demonstrate a real prototype on FPGAs or ASICs

Thank you! Questions?

MatRaptor: A Sparse-Sparse Matrix Multiplication Accelerator Based On Row-Wise Product

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