Nitish Kumar Srivastava

Apt 5G, 319 Highland Road, Ithaca, NY nks45@cornell.edu https://nitish2112.github.io/

Education

Ph.D. candidate, ECE, Cornell University *Aug'14-present*
Advisors: Prof. David Albonesi & Prof. Zhiru Zhang
CGPA: 4.01/4.0

B.Tech, EE, Indian Institute of Technology, Kanpur *July'10-May'14*
Institute Rank 1, GPA: 10/10

Research

Hardware Software Co-design for Accelerating Sparse and Dense Tensor Algebra *Oct'16*
Under Dr. David Albonesi, Dr. Zhiru Zhang and Dr. Christopher Batten, ECE, Cornell University
- Designing a storage formats and hardware accelerator for sparse and dense tensor algebra.
- Implementing the design on FPGA for prototyping.

Halide-based Compiler for Accelerating Dense Tensor Computations on FPGA *July'18*
Under Dr. Hongbo Rong, Intel Parallel Computing Lab, Dr. Zhiru Zhang, ECE, Cornell University
- Creating a language and compiler for generating spatial hardware for dense tensor computations.
- SGEMM design with 10 lines of code generates a FPGA design which matches peformance of Altera IP.

Operation Dependent Frequency Scaling using Desynchronization *June'15*
Under Dr. Rajit Manohar, ECE, Cornell University
- Designed efficient clock network using asynchronous handshakes to dynamically scale the frequency.
- Can scale frequency of processors every cycle based on dynamic instruction stream.

Accelerating Face Detection on Programmable SoC Using HLS *Jan'15*
Under Dr. Zhiru Zhang, ECE, Cornell University
- Designed accelerator for Viola Jones face detection algorithm using High Level Synthesis.
- Able to achieve a frame rate of more than 30 fps suitable for realtime applications.

Publications

- **Productively Generating High-Performance Spatial Hardware for Tensor Computations**
Nitish Srivastava, Hongbo Rong, Zhiru Zhang, etc. (submitted to FCCM 2019)
- **Operation Dependent Frequency Scaling using Desynchronization**
Nitish Srivastava and Rajit Manohar, IEEE, Transactions on VLSI systems (TVLSI), 2019
- **Rosetta: A Realistic HLS Benchmark Suite for Software Programmable FPGAs**
Y. Zhou, U. Gupta, S. Dai, R. Zhao, N. Srivastava, H. Jin et.al. Int'l Symposium on FPGAs, 2018
- **Accelerating Face Detection on Programmable SoC Using C-Based Synthesis.**
Nitish Srivastava, Steve Dai, Rajit Manohar and Zhiru Zhang, Int'l Symposium on FPGAs, 2017
- **Flexible and dynamic power allocation in broadband multi-beam satellites.**
Nitish Srivastava, and A. K. Chaturvedi, IEEE Communications Letters, 2013

Patents

Operation Dependent Frequency Scaling using Desynchronization (under process)

Selected Awards

- Selected as a **Cornell Fellow** in 2014 for outstanding academic performance.
- **President's Gold Medal** for best academic performance in the graduating batch, 2014.
- **Proficiency Medal** and **Pratik Mishra Gold Medal** for the best performance in ECE 2014.
- Awarded **Viterbi scholarship** (20 selections all over India) in 2013.
- **All India Rank (AIR) 364(99.99 percentile)** in IIT JEE'10.

Technical Skills

Hardware Verilog, Vivado HLS, Altera Opencl, BSV, Synopsys CAD tools, gem5
Software Halide, C, C++, Python, Java, MATLAB, OpenMP, MPI, CUDA, Opencl

Relevant Courses

Computer Architecture	Operating Systems	Compilers
Parallel Computing	Analysis of Algorithm	Machine Learning